Analog Design

- Electronic Design Automation Tools and Foundry Access
- Analog CMOS Circuit Design
- Packaging, Interconnect and Systems Issues

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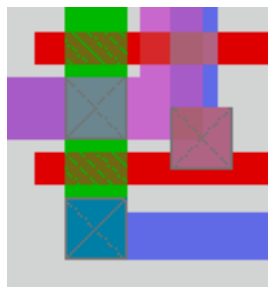
Electronic Design Automation (EDA)

- Commercial: Cadence, Mentor, Synopsys, Tanner
- Public domain: http://www-cad.eecs.berkeley.edu/software.html is a good starting point. See also http://bach.ece.jhu.edu/~tim/programs/magic/ for Magic, a VLSI Layout Editor.

cadence

Magic VLSI Layout Tool
Current distribution version 7.1



Mentor Graphics

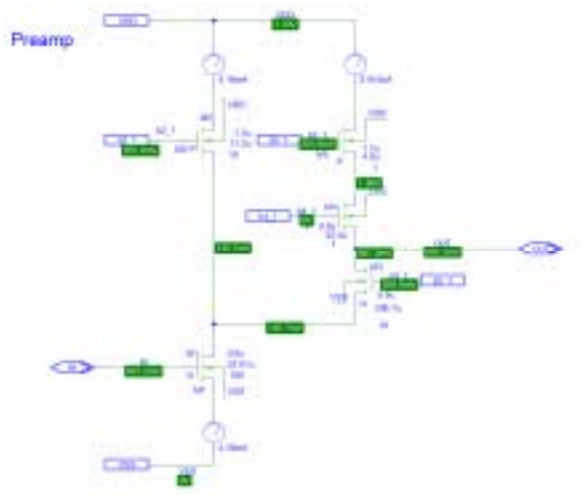
SYNOPSYS

Tanner EDA

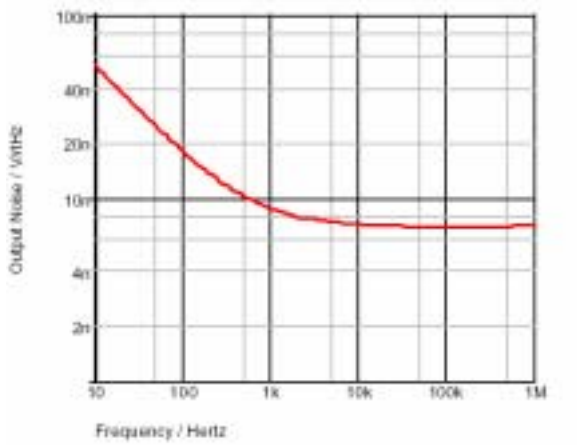
Essential tools for circuit-level design

- Transistor-level circuit simulator
  - *Matrix solution of network equations of your circuit*
  - *PSPICE, HSPICE, SPECTRE are the standards*
  - *inputs: circuit topology, device models, source driving functions*
  - *Outputs:*
  - *DC bias point, source sweep, temperature sweep*
  - *Frequency sweep using linearized model of active devices*
  - *Noise analysis in freq. domain*
  - *Time sweep*
  - *Monte-Carlo facility, samples from user-defined parameter distributions*
- Transistor models
  - *Strike a balance between*
    - Accurate in all transistor operating regions
    - Physics-based
      - Surface-potential based
      - Inversion charge based
    - Computational efficiency
    - Simple parameter extraction methodology
  - *Recent interest in high frequency CMOS design for RF applications has led to improved analog models*
  - *BSIM, EKV, MOS9 for advanced CMOS*
  - *Usually supplied by foundry*

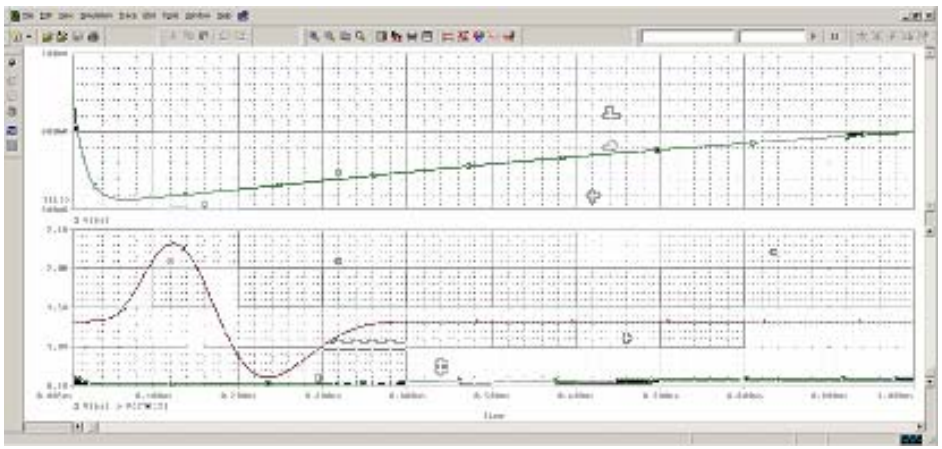
SPICE input & outputs



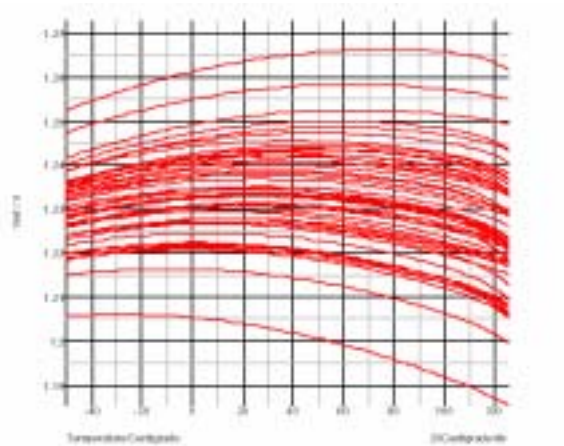
Schematic entry with backannotated node voltages and currents



Noise analysis: equivalent input noise density vs. frequency



Transient analysis result: voltages vs. time

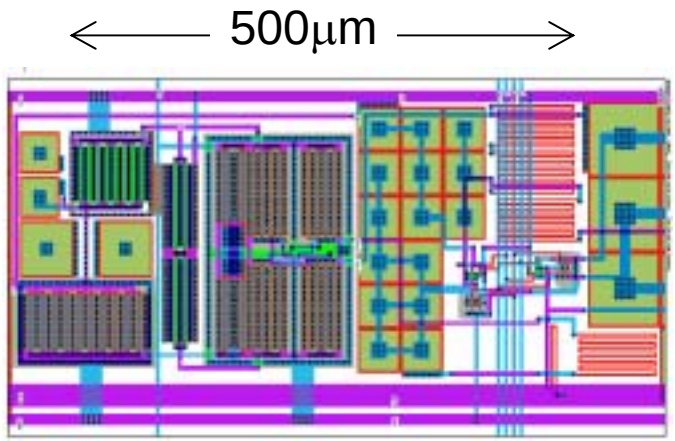


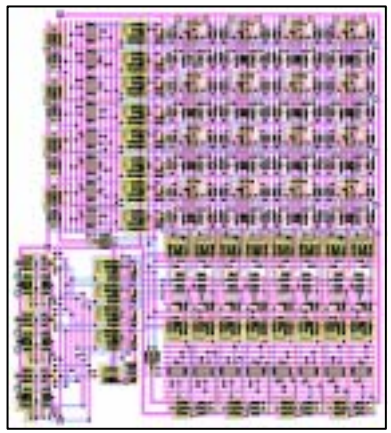
Monte Carlo analysis: node voltage vs. temperature, 50 runs from parameter distribution

EDA tools for physical design

- Chip layout (full custom, no pre-designed blocks)
  - *Polygon-level mask editor with built-in process knowledge*
- Design rule checker
  - *Checks mask geometry, flags violations of foundry design rules*
- Connectivity verification
  - *Layout-to-schematic network comparison*
- Parasitic extraction
  - *Find capacitance, resistance associated with interconnect lines on chip*

Layout with MAGIC

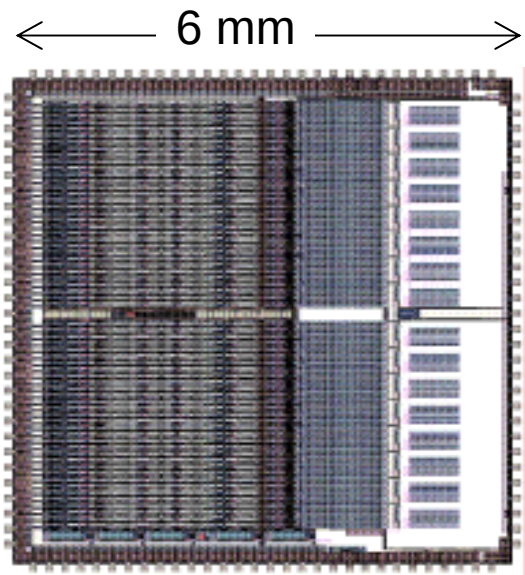




Analog and digital layout, 1.2μm CMOS

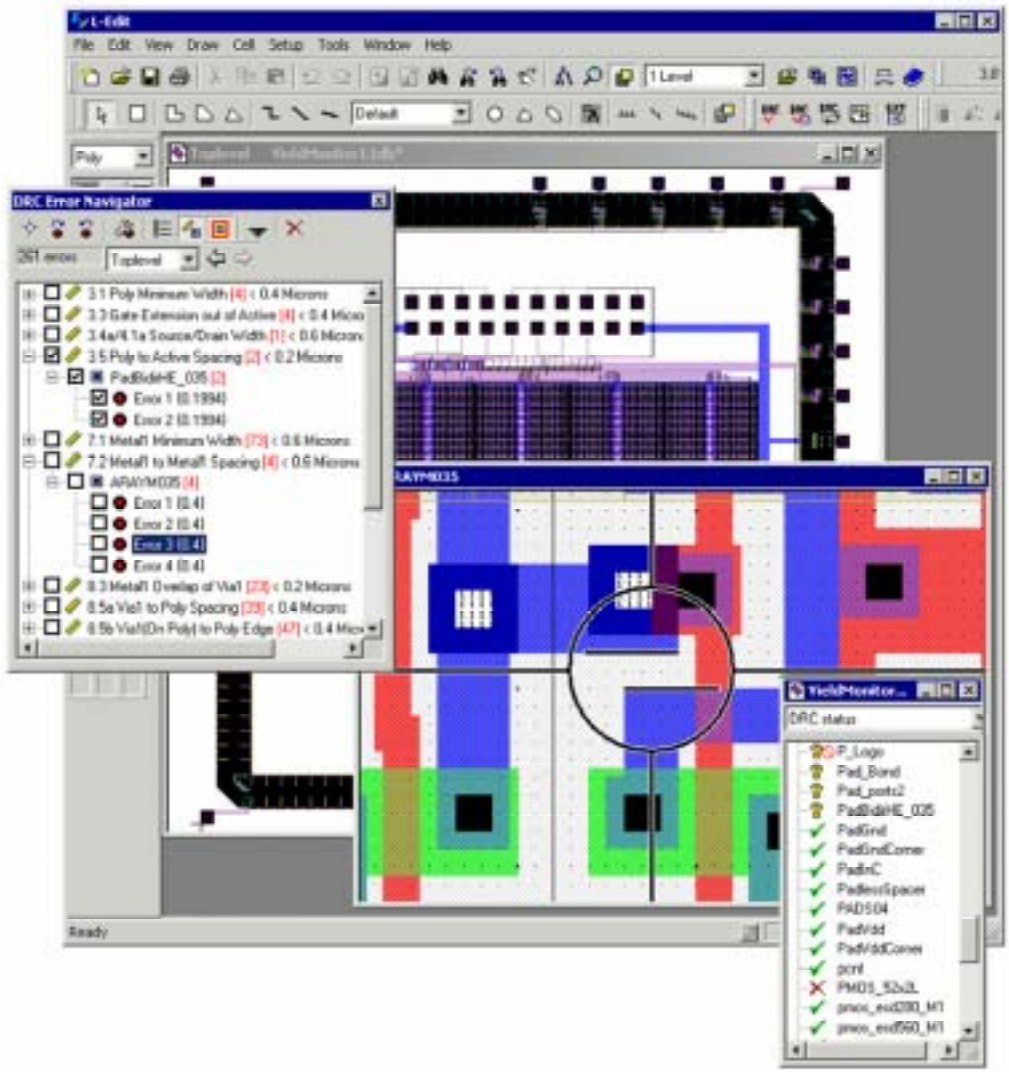
```
****** top level cell is ./preampflat.ext
C1 IN 2 5.00932e-13
Cxxnull 2  vss  1.323e-13
M1  BGND  IN  1  GND!  nch M=48  W=87.6U L=1.2U GEO=3
M2  1  VB1  Vdd  Vdd  pch M=2  W=42.0U L=3.0U GEO=3
M3  3  VB1  Vdd  Vdd  pch  W=30.0U L=3.0U GEO=3
M4  VSS  2  3  Vdd  pch  W=12.0U L=1.8U GEO=3
M5  2  BGND  1  Vdd  pch M=6  W=83.4U L=1.2U GEO=3
M6  2  VB2  VSS  GND!  nch  W=199.8U L=40.2U GEO=3
M7  VSS  VB2  OUT  GND!  nch M=3  W=199.8U L=40.2U GEO=3
M8  OUT  3  Vdd  GND!  nch M=24  W=87.6U L=1.2U GEO=3
R1 IN 3 57166.5
C3  9_2072_18#  OUT  1.0F
C4  9_226_18#  BGND  1.0F
C5  1  VSS  2.3F
C6  BGND  IN  8.6F
C7  Vdd  3  3.0F
C8  9_720_18#  BGND  1.0F
C9  1  IN  5.3F
C10  BGND  Vdd  1.8F
C11  OUT  3  4.2F
C12  Vdd  VSS  1.1F
C13  OUT  VB2  3.8F
C14  VSS  VB2  6.2F
C15  9_1806_18#  OUT  1.0F
C16  OUT  VSS  2.6F
C17  BGND  VSS  4.3F
C18  Vdd  VB1  1.1F
C19  1  GND 404.4F
C20  2  GND 79.6F
C21  3  GND 98.5F
C22  9_2072_18#  GND 1.0F
C23  VSS  GND 439.1F
C24  Vdd  GND 447.6F
C25  BGND  GND 449.7F
C26  9_226_18#  GND 1.0F
C27  9_720_18#  GND 1.0F
C28  OUT  GND 275.9F
C29  IN  GND 149.9F
C30  9_1806_18#  GND 1.0F
C31  VB1  GND 23.2F
C32  VB2  GND 96.3F
.END
```

Circuit netlist extracted from layout w/ parasitic capacitances



Mixed-signal circuit, 6x10^5 transistors, 0.25μm CMOS

Graphical Design Rule Check



Multiproject services for low-cost prototyping

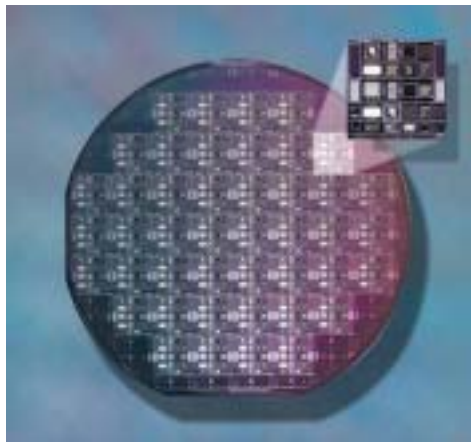
- Organize regularly-scheduled multiproject runs (MPW)
- Collect and merge designs and provide production-compatible masks to foundry
  - *share costs among users*
    - mask-area weighted
- Access to latest production processes from major foundries
  - *CMOS, BiCMOS, SiGe, (GaAs, InP, MEMS)*
- User support:
  - *design kit*
  - *models*
  - *parametric process data*
    - process control monitor and reference design probed after each MPW run
    - statistical process database
    - quality/yield monitor
  - *access to wafer thinning, dicing, wirebonding, and packaging services*
  - *low-volume production*

Multiproject services

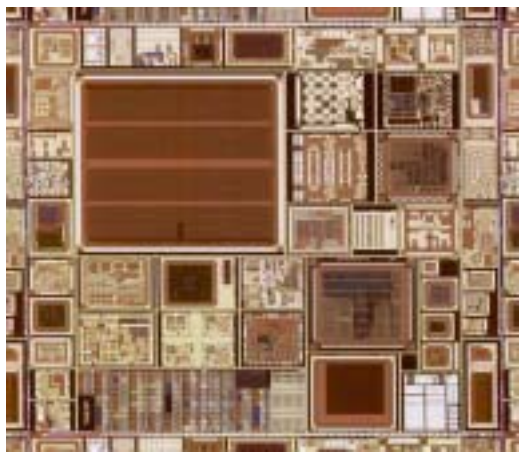
- Multi-foundry:
  - *MOSIS* *www.mosis.org*
  - *Europractice* *www.imec.be/europractice*
  - *Canadian Microelectronics Corp.* *www.cmc.ca*
- Foundry-based:
  - *TSMC* *www.tsmc.com*
  - *XFAB* *www.xfab.com*
  - *Zfoundry* *www.zfoundry.com*
  - *Jazz Semicond.* *www.jazzsemi.com*

MPW exampes

wafer



reticle (0.18μm CMOS)



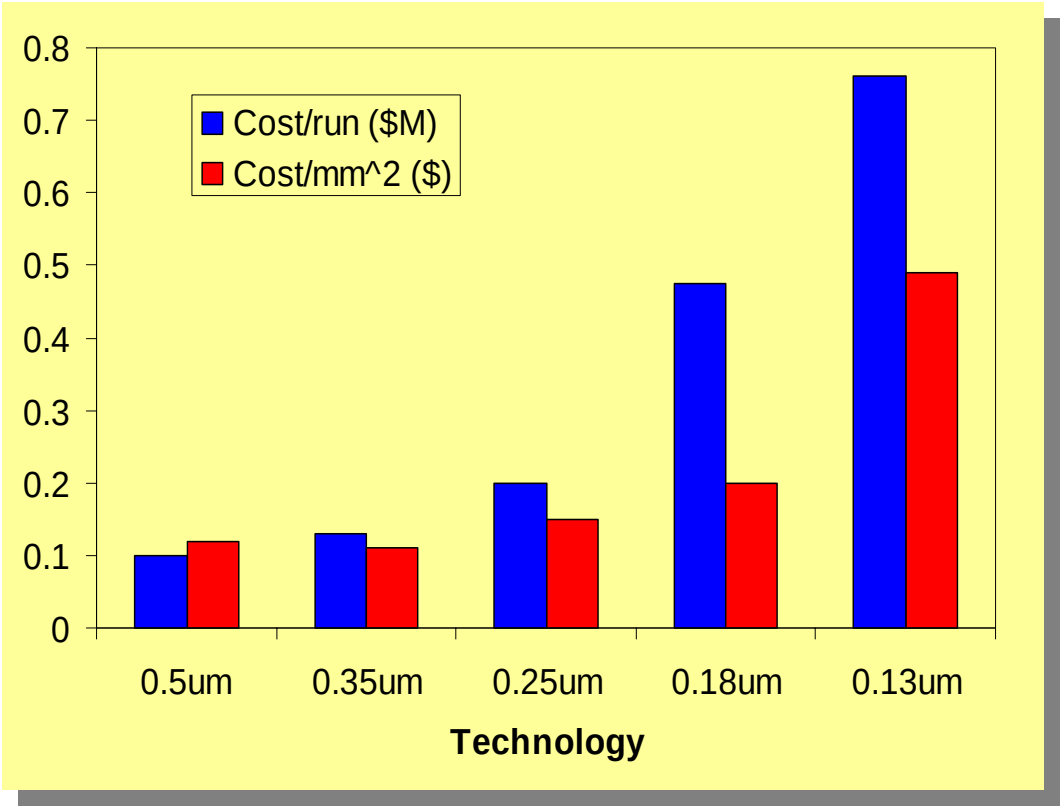
Cost comparison

Process	chip size	lot size	cost
	mm²	no. parts	$K
1.5μm CMOS	5	5	1.1
0.5μm CMOS	5	40	6.5
0.35μm CMOS	15	40	20.7
0.25μm CMOS mixed	25	40	47.3
0.18μm CMOS	50	40	126.8
0.35μm SiGe BiCMOS	50	40	90.0

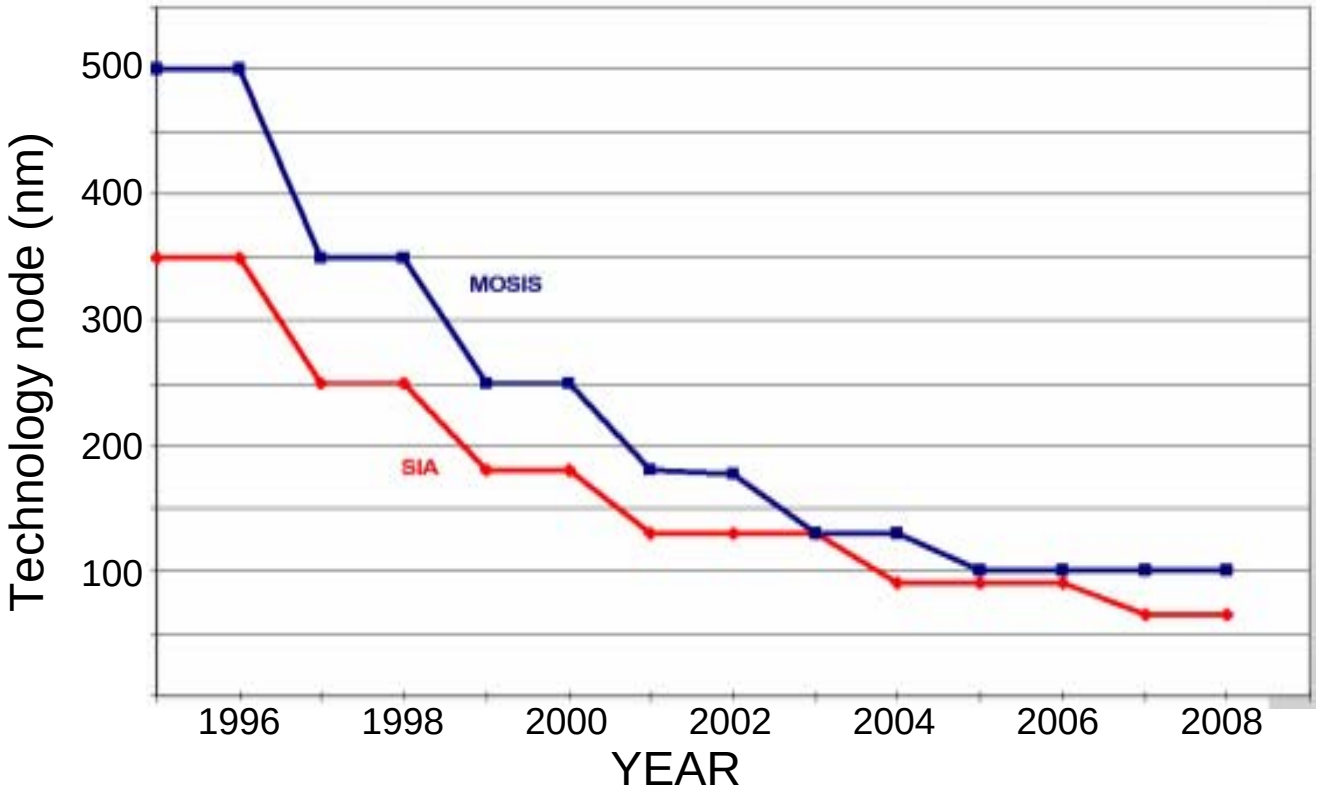
www.mosis.org

Engineering run costs

Typical engineering run = 20 wafers



Technology introduction roadmap
MOSIS and Semiconductor Industry Association



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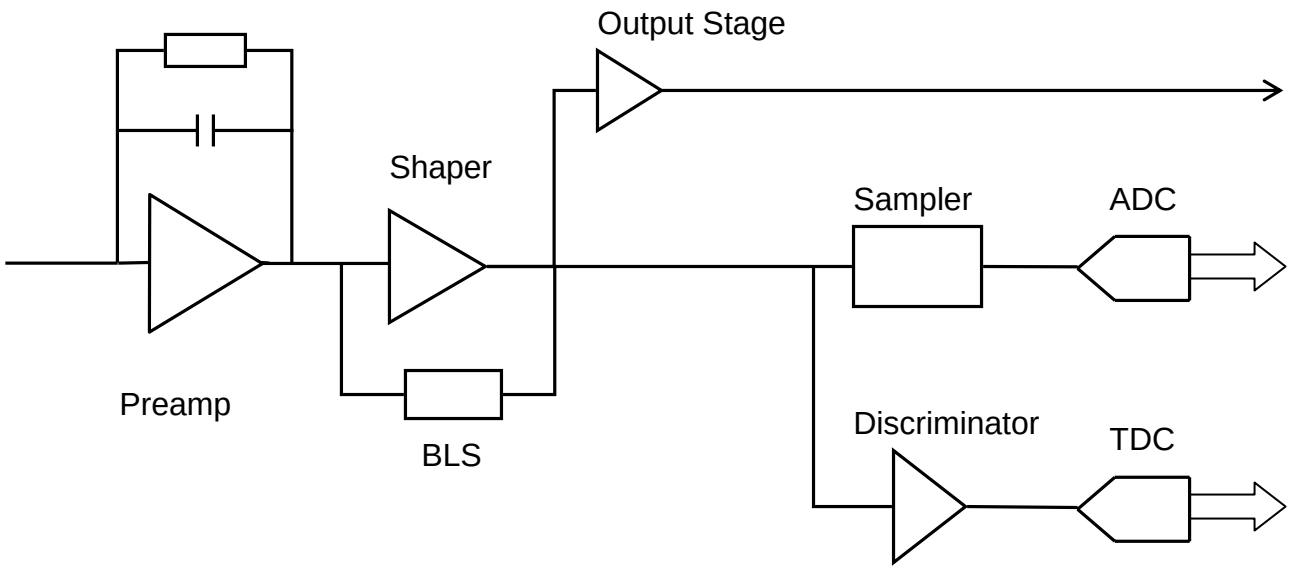
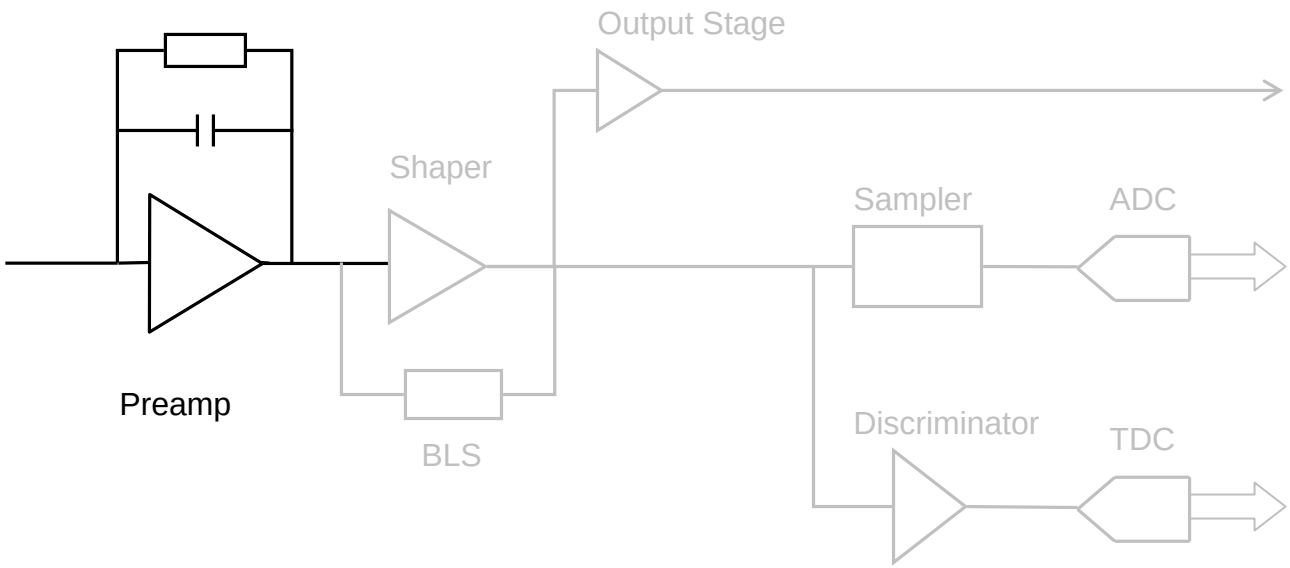
Signal Chain Block Diagram

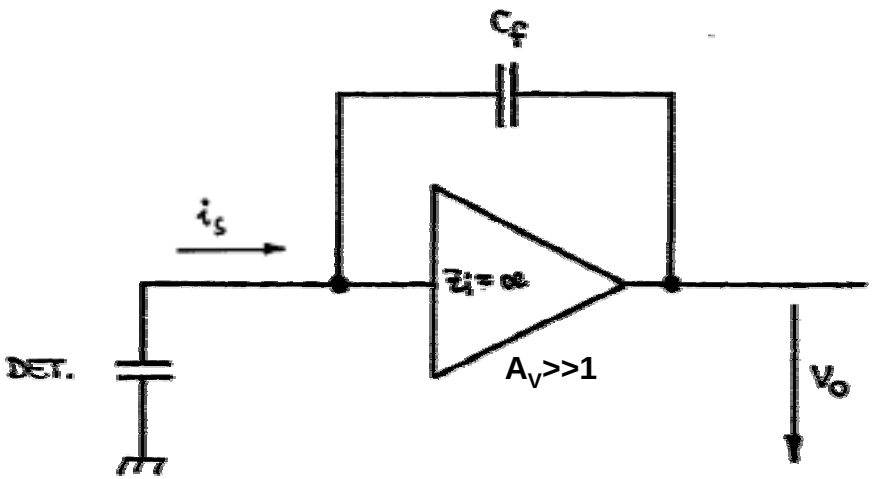


Charge Sensitive Preamplifier



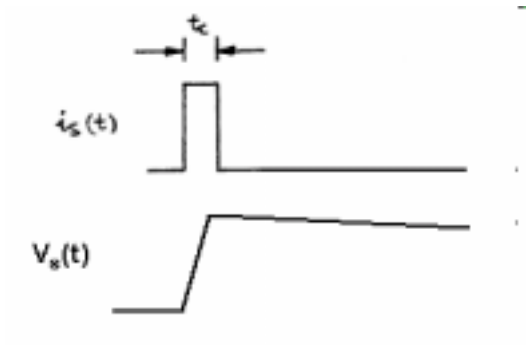
Low noise charge amplification

- Charge sensitive configuration (active integrator)



for $Z_{in}, |A_V| \to \infty$

$$V_s = \frac{\int i_s(t)dt}{C_f} = \frac{Q_s}{C_f}$$

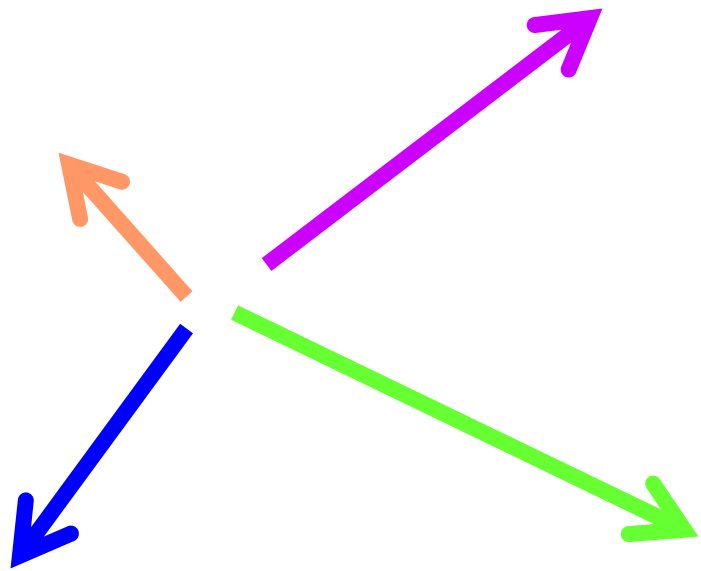


Gain insensitive to C_{det} and A_V

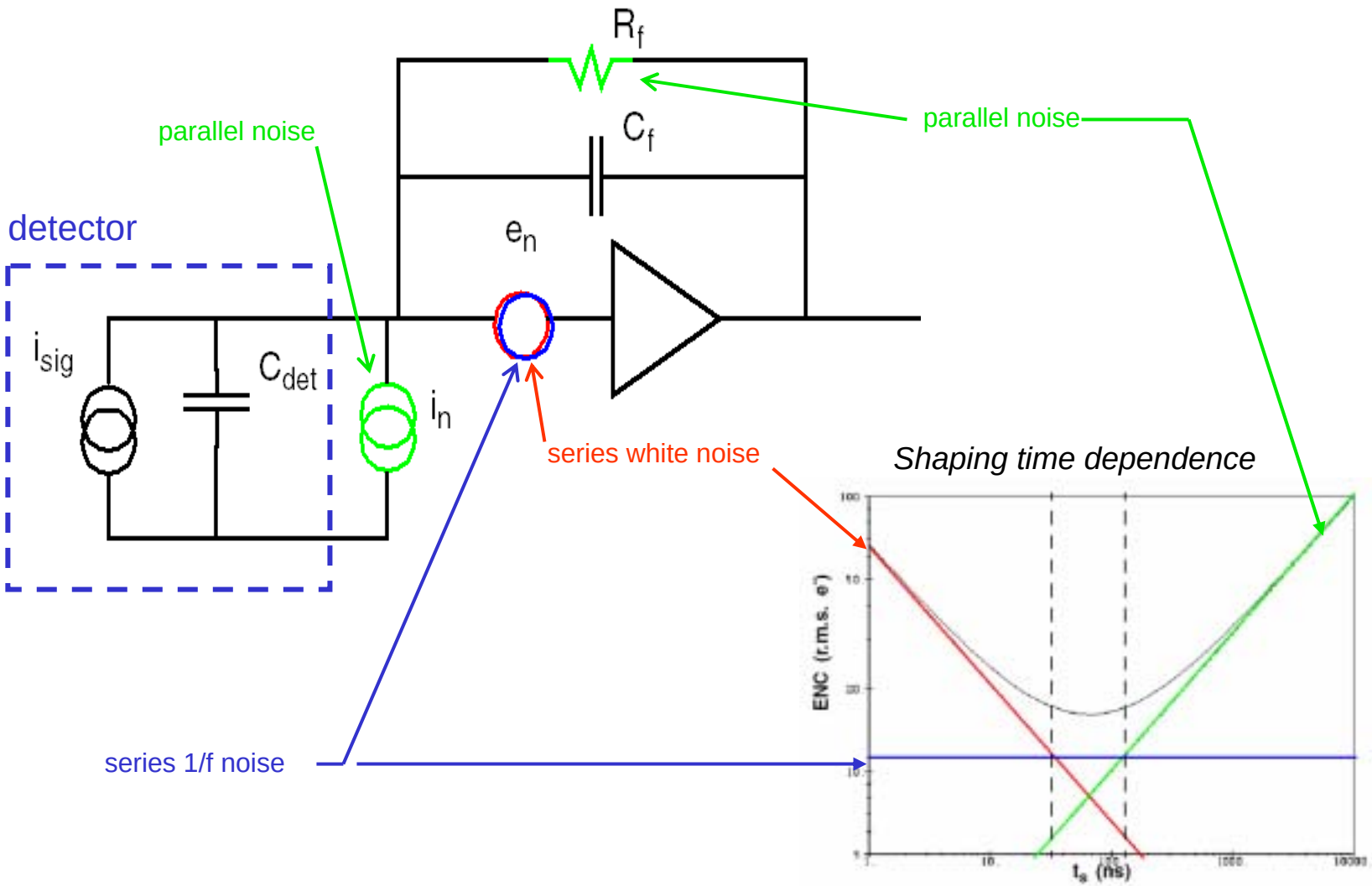
MOS charge amplifier design

- Key parameters:
  - C_{det} , I_{det} , Q_{max} *(detector)*
  - *Rate,* P_{diss} *(system)*
  - f_T , K_F , I_{in} *(technology)*

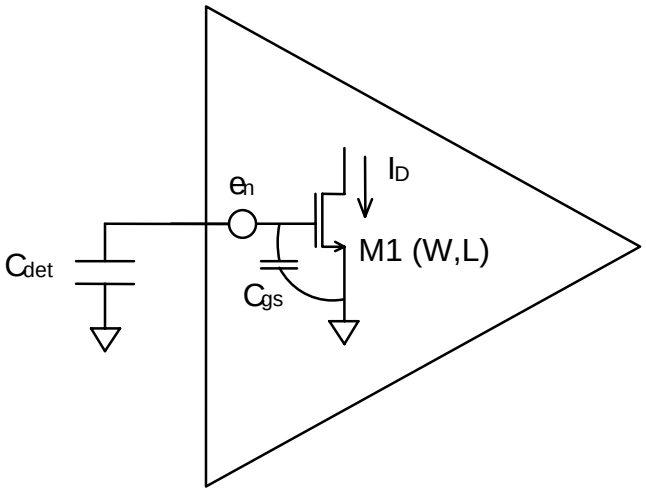
- Key design decisions
  - *NMOS/PMOS*
  - L_g
  - C_{gs}/C_{det}
  - *Reset system*
  - *Weighting function*



Charge amplifier noise sources



Dimensioning the input MOSFET for minimum noise



$$ENC^2 = \left(C_{det} + C_{gs}\right)^2 \cdot \left(\frac{4kT\gamma}{g_m \, t_m} + \frac{K_F}{C_{gs}}\right)$$

white 1/f

Choose minimum L for best g_m/C_{gs} ratio

Increasing M1 width makes e_n smaller while C_{gs} gets larger

$\Rightarrow$ ***optimum width for M1 must exist***

1/f noise:

$$C_{gs,opt} = C_{det}$$

White -- two cases :

I. Fixed V_{gs} (fixed current density, fixed f_T)

$$g_m \propto C_{gs}$$

$$C_{gs,opt} = C_{det}$$

II. Fixed I_D (practical case)

$$g_m \propto C_{gs}^{1/2} \text{ [strong inversion]}$$

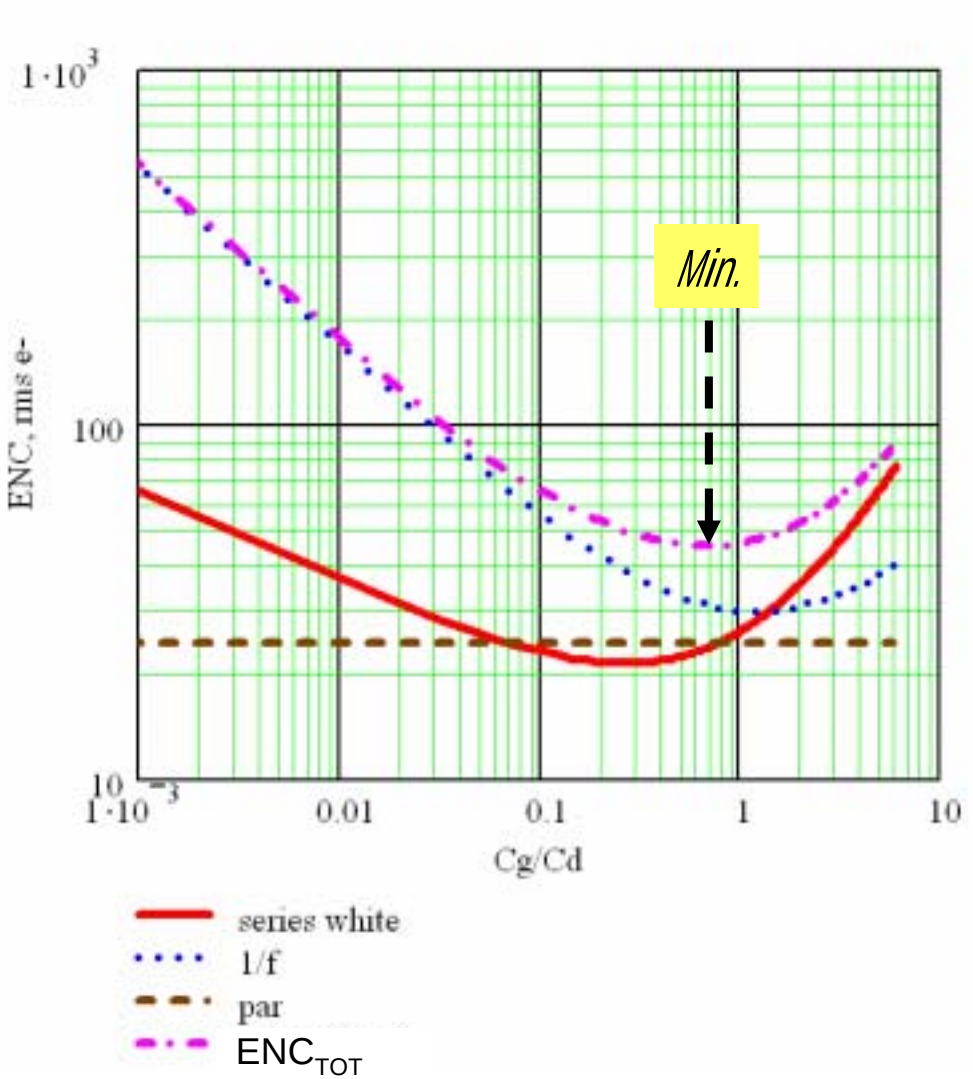
$$C_{gs,opt} = C_{det}/3$$

P. O'Connor, G. De Geronimo, "Prospects for charge sensitive amplifiers in scaled CMOS", NIM A480 (2002), 713 - 725

Composite noise

- C_{det} = 3 pF
- t_p = 0.5 μs
- P_{diss} = 1 mW
- I_{leak} = 100 pA
- Technology: 0.35 μm NMOS

- *Optimum width for series noise is a compromise between white and 1/f components*



Optimizing the input MOSFET using advanced models

Series noise "capacitive match" problem:

$$ENC^2 = ENC_{sw}^2 + ENC_f^2$$

$$ENC_{sw}^2 = \frac{a_1}{2\tau_p} e_{n,sw}^2 (C_d + C_{in})^2$$

$$e_{n,sw}^2 = \frac{4kTn\gamma}{g_m}$$

$$ENC_f^2 = a_2 \pi \frac{K_F}{C_{ox} WL} (C_d + C_{in})^2$$

γ and g_m depend on region of operation:

	γ	g_m
weak	1/2	qI_D / nkT
strong	2/3	$\sqrt{2\mu C_{ox} \frac{W}{L} I_D}$

How to handle moderate inversion?

G.De Geronimo, P.O'Connor , V. Radeka and B. Yu, "Front-end electronics for imaging detectors", *Nuclear Instrum. Methods* A471 (2001) 192-199

P. O'Connor and G.De Geronimo, "Prospects for charge sensitive amplifiers in scaled CMOS", *Nuclear Instrum. Methods* A484 (2002) 713-725

L. Fabris, P. Manfredi, "Optimization of front-end design in imaging and spectrometry applications with room temperature semiconductor detectors", *IEEE Trans Nucl. Sci*., 49 (4) ,1978 –1985, Aug. 2002

M. Manghisoni, L. Ratti, V. Re, and V. Speziali, "Submicron CMOS Technologies for Low-Noise Analog Front-End Circuits", *IEEE Trans. Nucl. Sci.* 49,1783-1790, Aug. 2002

Simplified EKV model for hand calculations

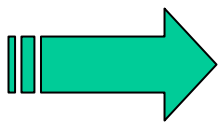
- substrate-referenced compact MOS model
- small, physics-based parameter set
- continuous modeling of weak to strong inversion
- simple set of equations valid for saturation:

Inversion coefficient $i = I_D / I_0$

$$I_0 = 2n\beta \cdot U_T^2 \qquad \beta = \mu \cdot C_{ox} \frac{W}{L} \qquad U_T = \frac{kT}{q}$$

Interpolation function :

$$f(i) = \frac{1}{2}\left(\sqrt{1+4i}+1\right)$$



$$\frac{g_m}{I_D} = \frac{1}{n \cdot U_T} \frac{1}{f(i)}$$

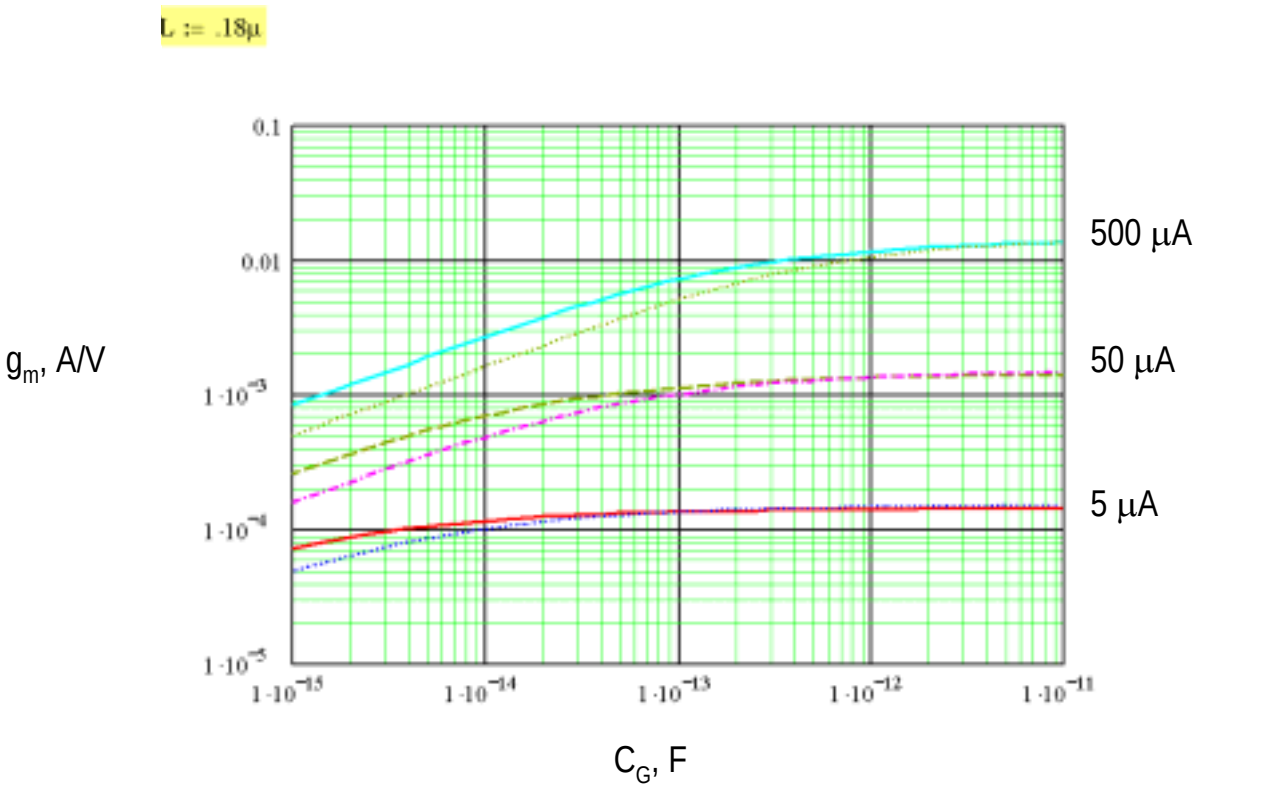
$$\frac{C_{GS}}{WLC_{ox}} = \frac{1}{\frac{3}{2} + \frac{f(i)}{i}}$$

$$\frac{S_{th}}{4kTng_m} = \frac{\frac{1}{2} + \frac{2}{3}i}{1+i} \equiv \gamma$$

short-channel effects not modeled

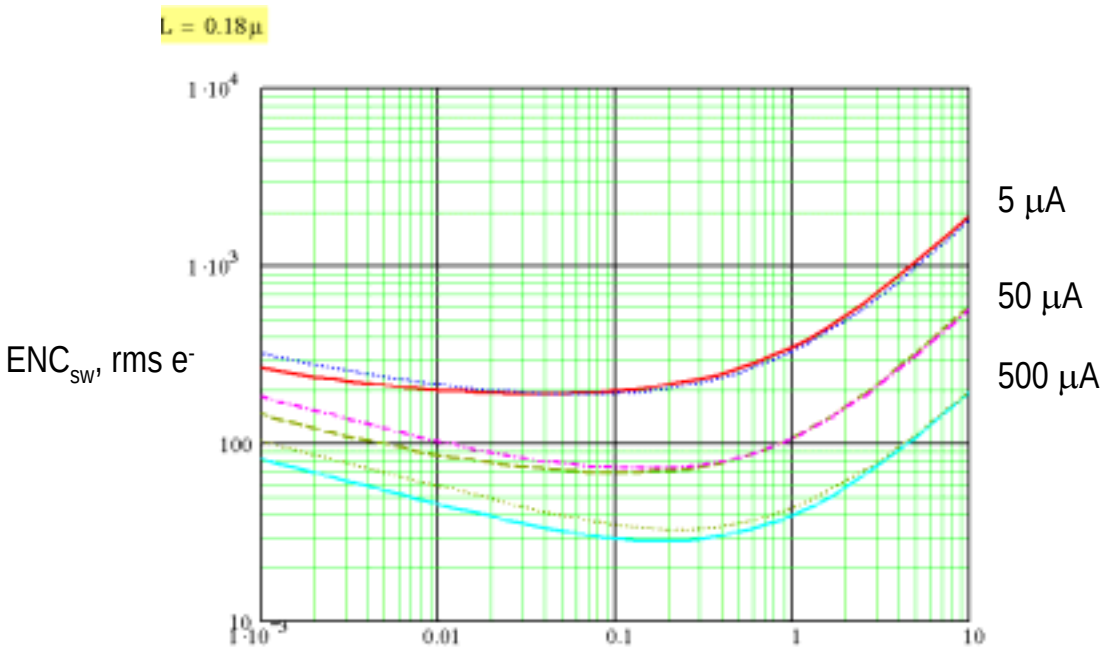
C. Enz, F. Krummenacher, E. Vittoz, "An Analytical MOS Transistor model valid in all regions of operation and dedicated to low-voltage and low-current applications", *Analog Integrated Circuits and Signal Processing* 8, 83-114 (June 1995)

g_m vs. C_G vs. scaling



NMOS (upper) PMOS (lower)

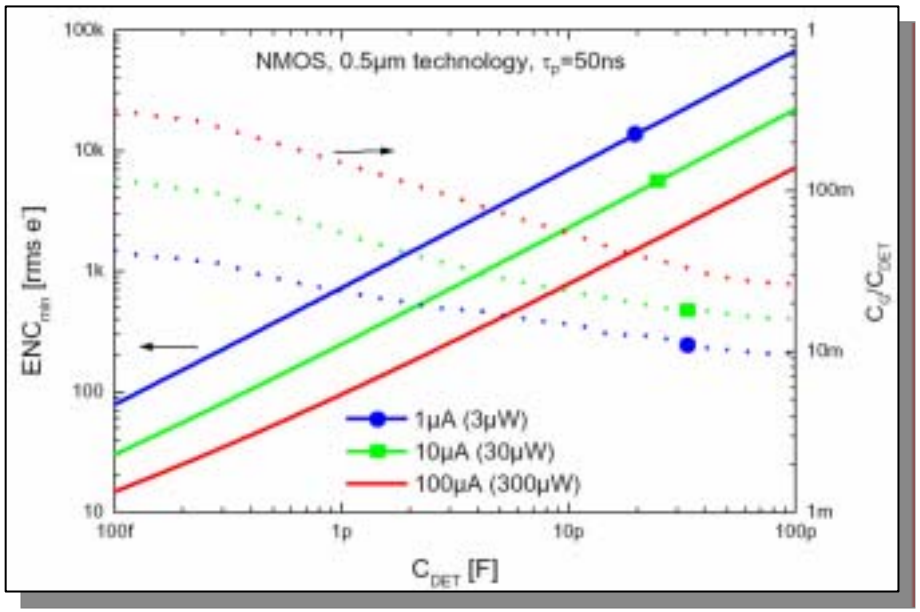
White series noise vs. C_G/C_d vs. scaling



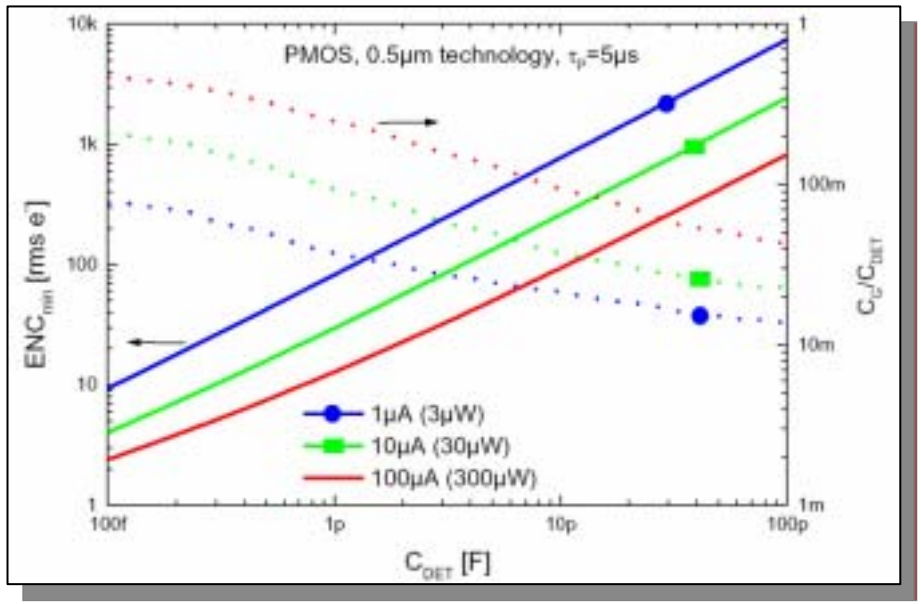
NMOS (upper) PMOS (lower)

White series ENC, $C_{G,opt}/C_{DET}$ vs. C_{DET}

NMOS



PMOS



For fixed power budget,

$$ENC \propto \begin{cases} C_{DET}, \text{ weak inversion} \\ C_{DET}^{3/4}, \text{ strong inversion} \end{cases}$$

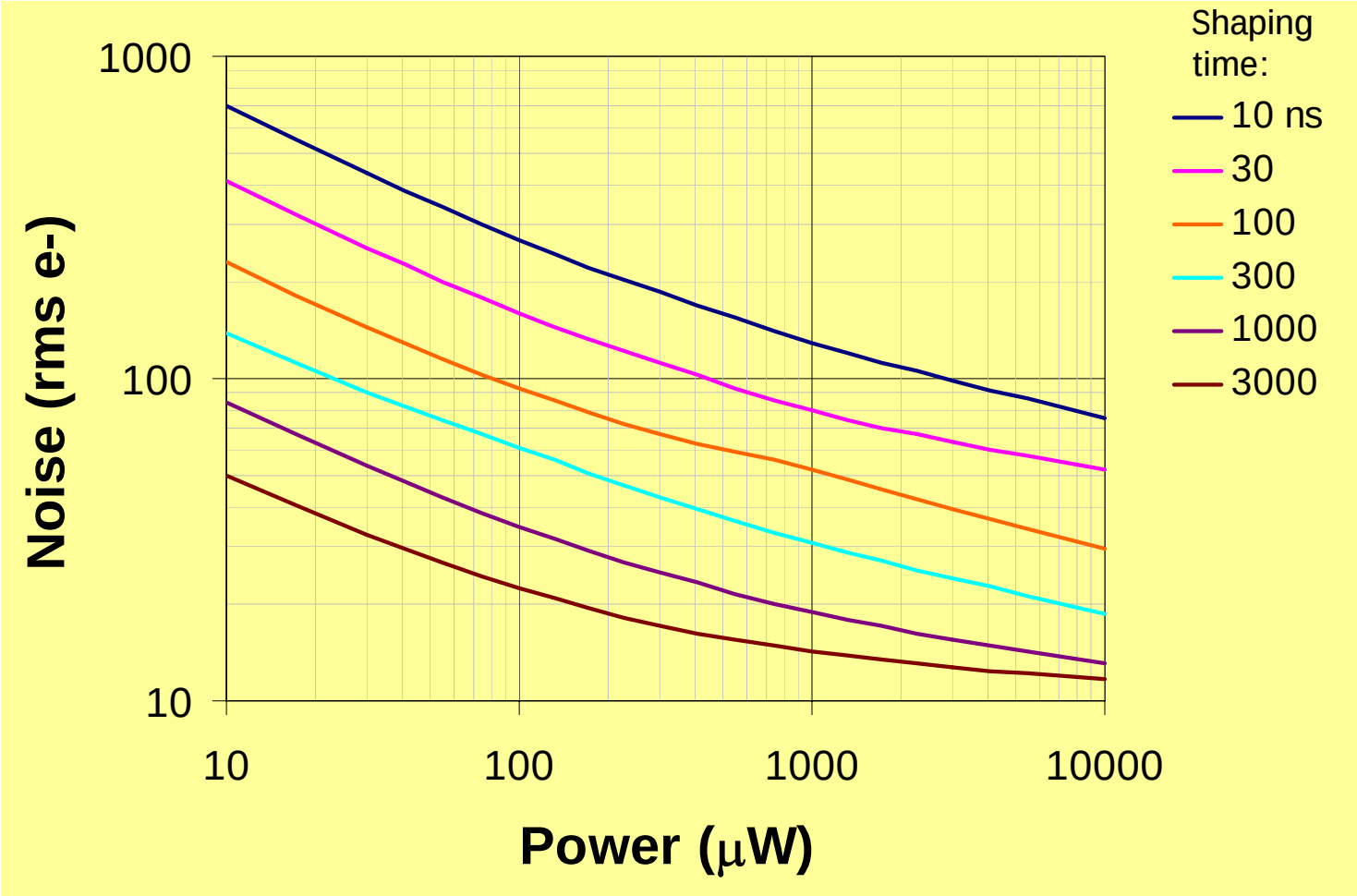
Power allowed to scale with C_{DET}:

$$ENC \propto C_{DET}^{1/2}$$

De Geronimo et al. , NIM A 471 (2001) 192 - 199

Optimized noise vs. power

(MOSFET optimized at each power level and shaping time)

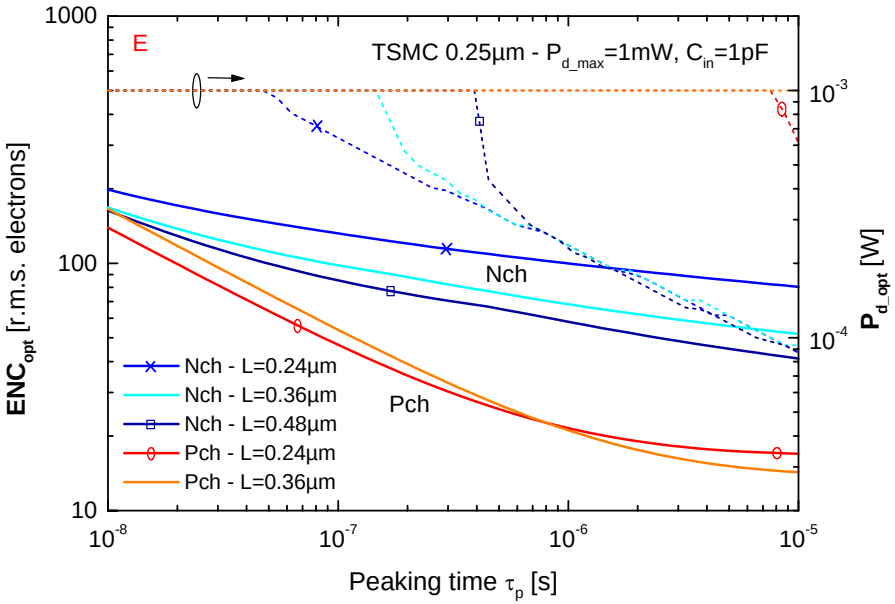


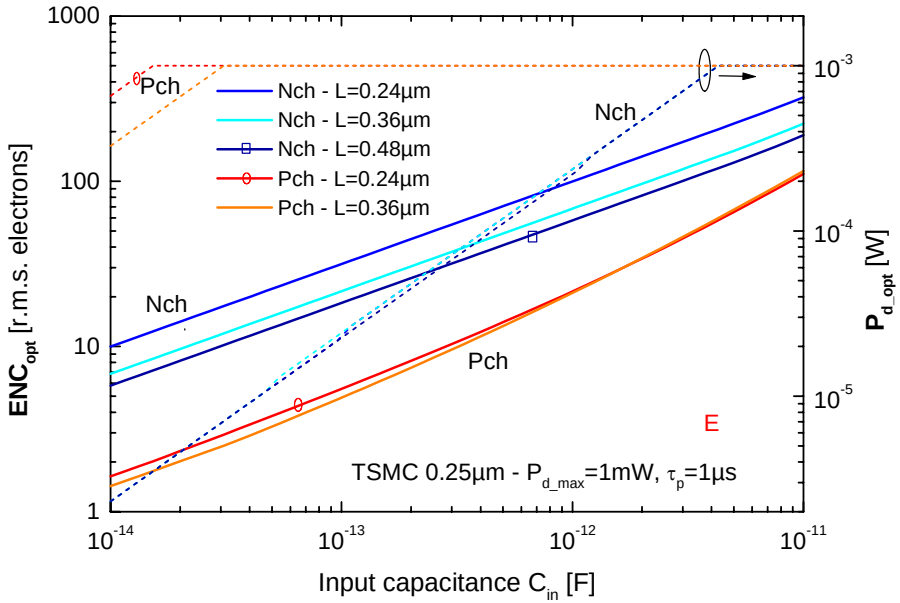
Note:

$$\left|\frac{dN}{dP}\right| \leq 0.4$$

Cd = 1pF
0.25 μm CMOS

0.25μm CMOS optimized noise/power





Enhanced noise model incorporates:

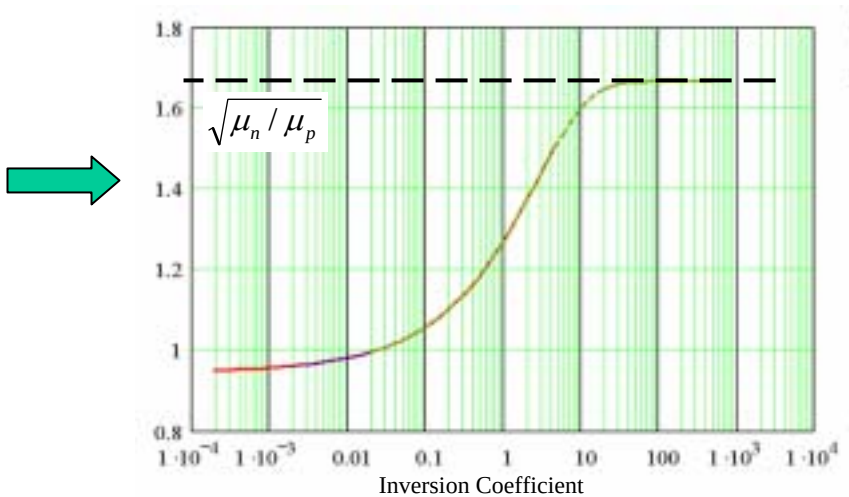
- *Gate capacitance bias dependence*
- *Gate-source and gate-drain overlap capacitance*
- *Length-dependent 1/f noise coefficient*
- *1/f$^{\alpha}$ behavior of low-frequency noise*

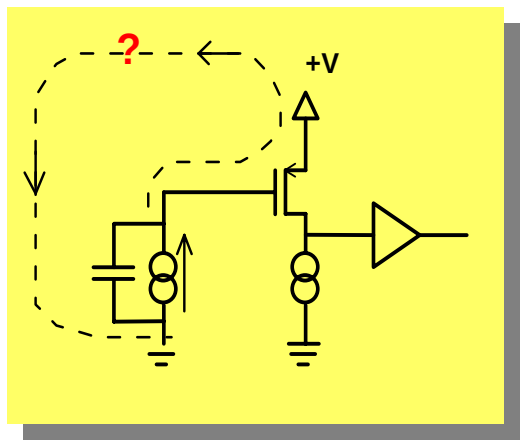
G. De Geronimo, P. O'Connor, to be published in IEEE Trans. Nuc. Sci.

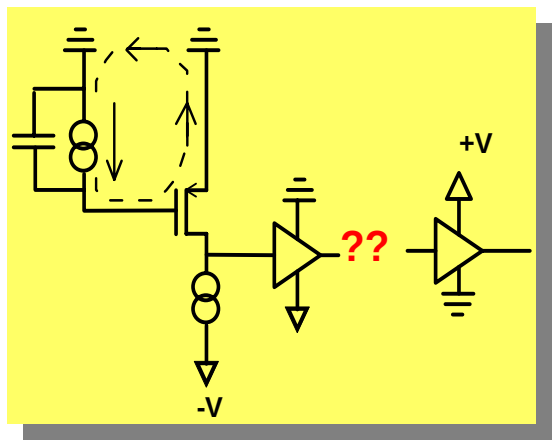
Choice of PMOS vs. NMOS

- *PMOS lower 1/f noise*
- *NMOS white series noise advantage over PMOS diminishes each generation*
- *PMOS can be operated at reverse V_{BS} to reduce bulk resistance noise*
- *PMOS lower tunneling current at ultra-thin t_{ox}*
- *Single-supply operation of PMOS-input preamp awkward:*

g_{mn}/g_{mp} vs IC







Minimum series noise

- Input MOSFET fully optimized:

$$ENC_{sw,opt} \approx \sqrt{kTC_{\det}}\sqrt{\frac{\tau_{el}}{t_m}}$$

$$ENC_{1/f,opt} \approx \sqrt{K_F C_{\det}}$$

τ_{el} = electron transit time under the gate $= C_{gs} / g_m$

- Key ingredients for low series ENC:
  - *low* C_{det}
  - *long* t_m
  - *short* τ_{el}
  - *low* K_F

Gate resistance noise

- Polysilicon gate is resistive:
  - ρ_{poly} **25 Ω/sq.**
  - $\rho_{silicided\ poly}$ **4 Ω/sq.**

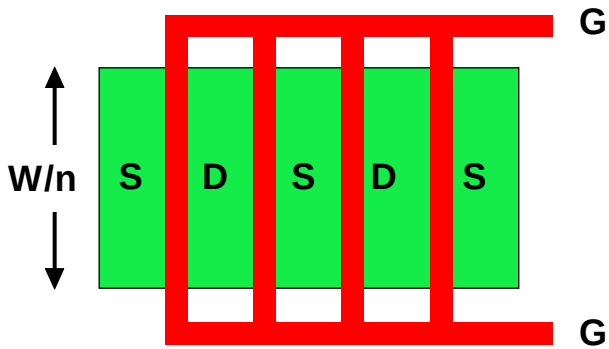
resistance of non-interdigitated gate:

$$R_g = \rho_{poly} \cdot \frac{W}{L}$$

series noise due to gate resistance:

$$e_{ng}^2 = 4kT \cdot R_{eq}$$

FET with interdigitated layout



n gate fingers
n = 4

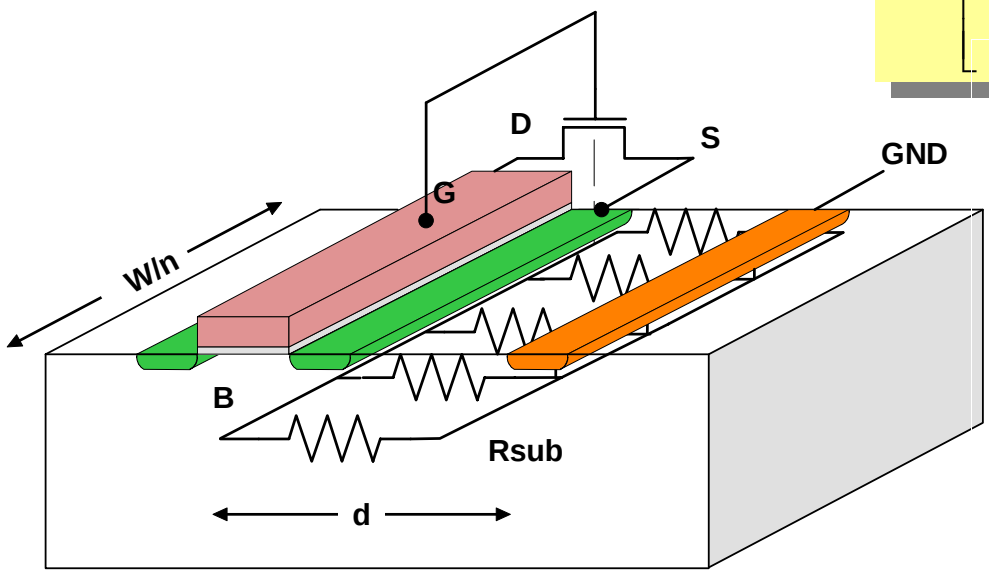
Layout	Req driven one end	Req driven both ends
Single finger	Rg/3	Rg/12
Interdigitated n fingers	Rg/3n^2	Rg/12n^2

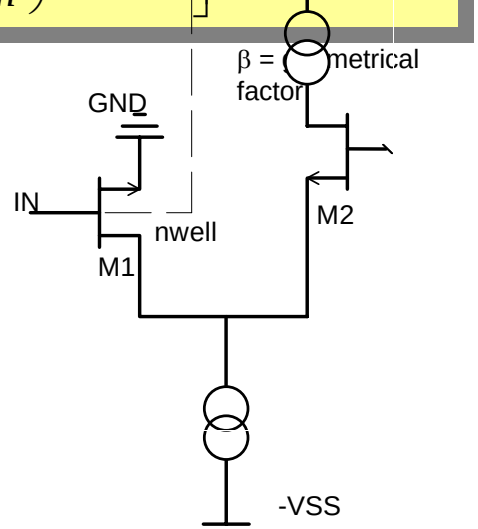
Bulk resistance noise

- Resistive substrate couples to the channel via the back transconductance g_{mb}.
- Substrate resistance is distributed.

leads to noise in the channel:

$$i_{db}^2 = \left[4kT \cdot n \cdot \beta \frac{d}{\left(\frac{W}{n}\right)} \cdot \left(\frac{g_{mb}}{n} \right)^2 \right] = 4kT\beta \frac{d}{W} g_{mb}^2$$

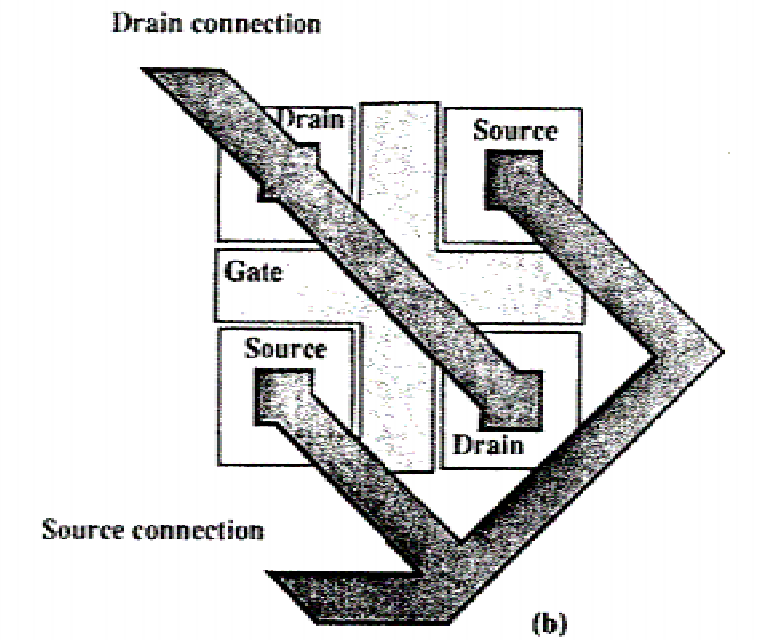




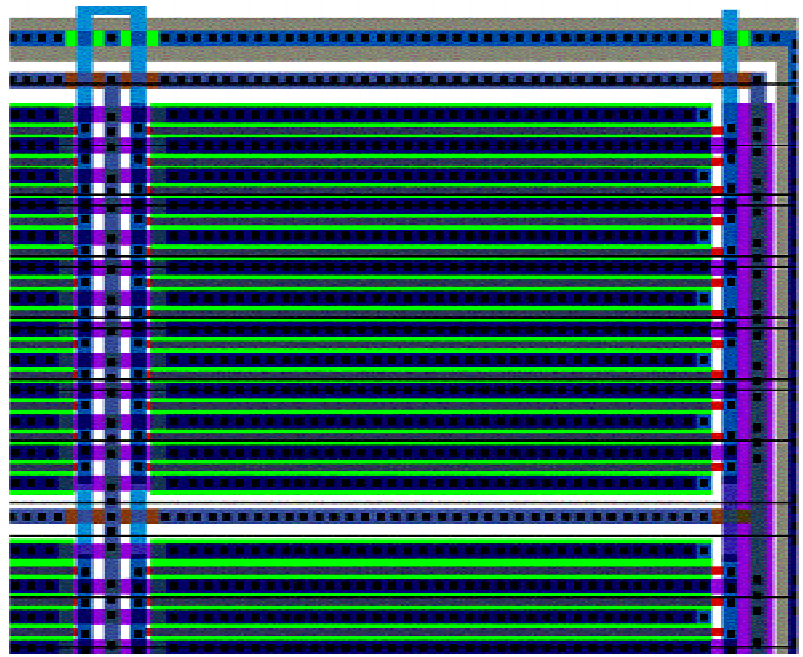
- Minimize by reverse biasing the source-substrate junction.

Layout techniques to reduce gate and bulk resistance noise

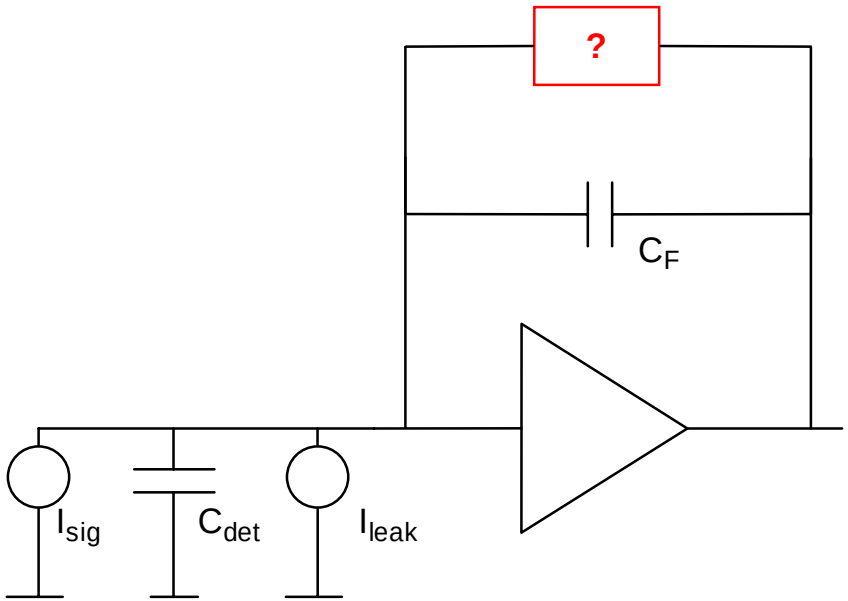
Waffle iron layout



Substrate contacts, guard ring, multiple gate fingers contacted on both ends

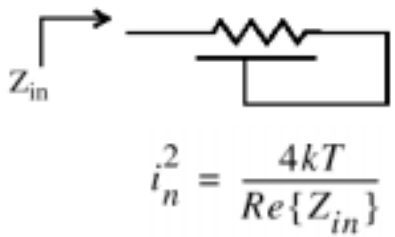


Preamp reset – requirements

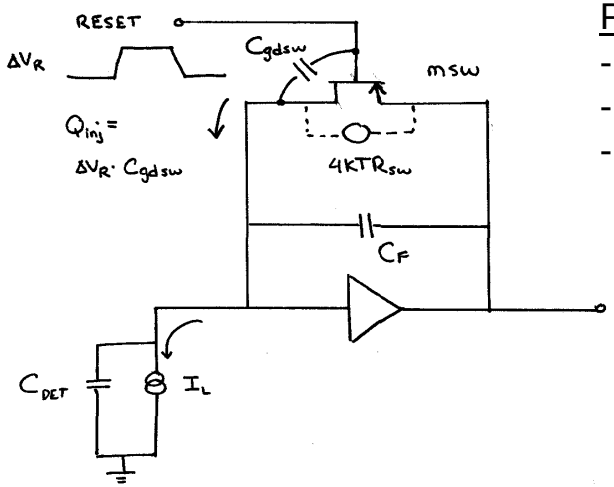


- all charge preamplifiers need DC feedback element to discharge the input node and stabilize the bias point
- usually, a resistor in the MΩ – GΩ range is used
- monolithic processes don't have high value resistors
- we need a circuit that behaves like a high resistor and is also
  - *insensitive to process, temperature, and supply variation*
  - *low capacitance*
  - *lowest possible noise*
  - *linear*

Preamplifier reset – monolithic techniques (1)



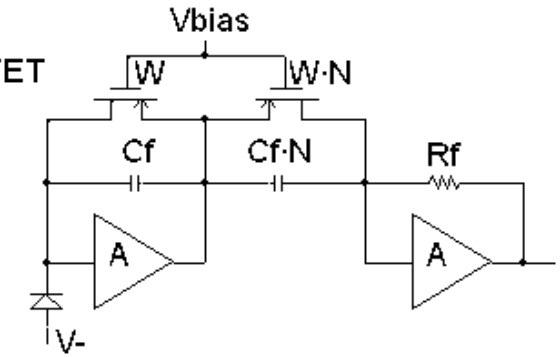
Physical resistor
- always accompanied by parasitic capacitance
- de-stabilizes circuit and increases noise
- noise higher than 4kT/R by factor ~ RC/t_m



Pulsed reset by MOS switch
- sampled noise $\sqrt{kTC_F}$
- Q_{inj} noise from switch control voltage
- leakage current integrates on output node $dV_{out}/dt = I_L/C_F$

Preamplifier reset – monolithic techniques (2)

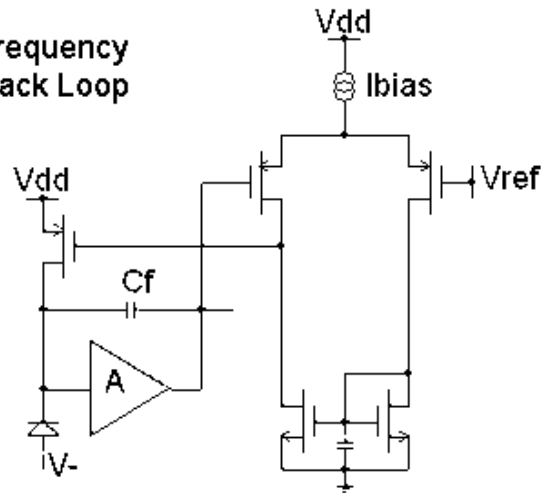
Single MOSFET



O'Connor et al., TNS v44 n3 (1997)
De Geronimo et al., NIM A421 (1999)
De Geronimo et al., TNS v47 n4 (2000)

- provides effective current gain -N
- full compensation (high linearity)
- minimum noise (thermal)
- requires baseline stabilization
- can be realized in multiple stages

Low Frequency Feedback Loop

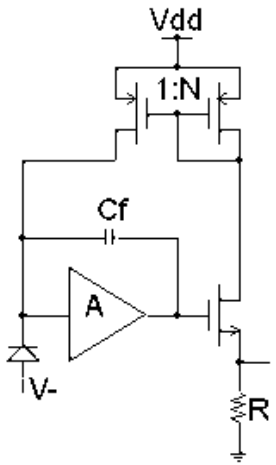


Krummenacher, NIM A350 (1991)
Ludewigt et al., TNS v41 n4, (1994)
Vandenbussche et al., TNS v45, n4 (1998)
Manfredi et al., Nucl.Phys.B 61B, Proc.Suppl. (1998)

- noise can be high
- requires baseline stabilization at high rates
- compensation an issue

Preamplifier reset – monolithic techniques (3)

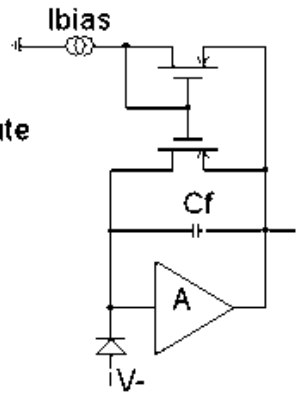
R-Scaling



Santiard et al., CERN-ECP/94-17 (1994)
Chase et al., NIM A409 (1998)
Sampietro et al., Elec.Lett. v34 n19 (1998)

- noise can be high (large values of R and N required)
- linearity an issue
- parasitic capacitor an issue
- compensation available in some configuraitions
- requires baseline stabilization

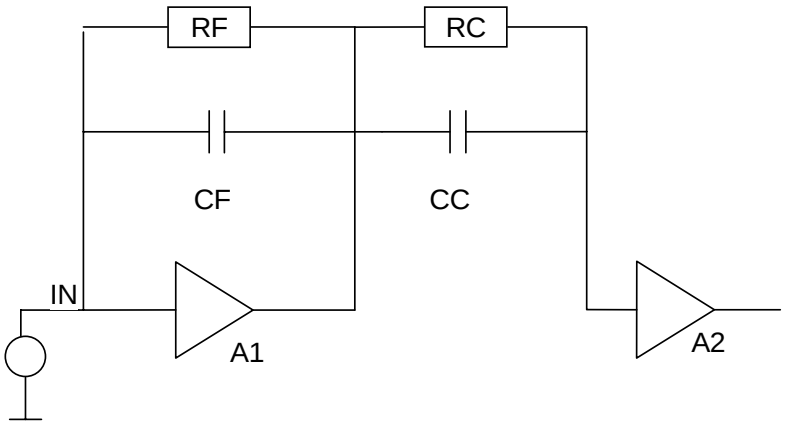
Slew-rate Limited



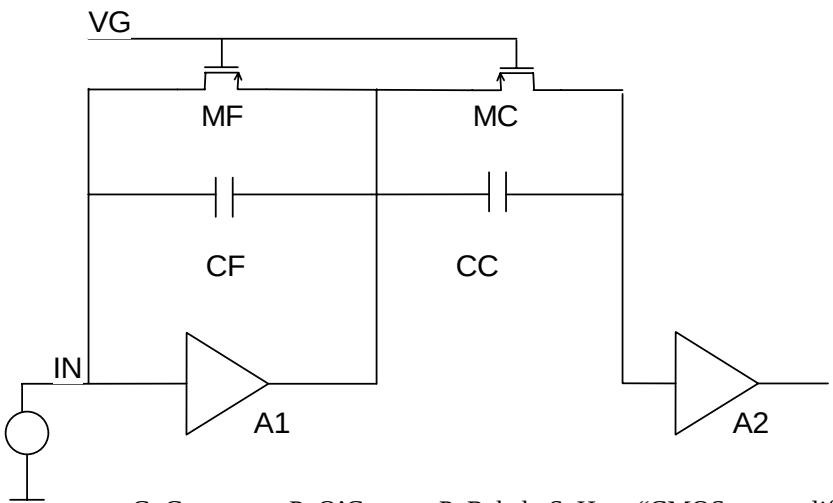
Blanquart et al., NIM A395 (1997)
Blanquart et al., NIM A439 (2000)

- MOSFET operates in saturation only when there is signal activity
- noise can be high (it requires Ibias > Idet)
- parasitic capacitor an issue
- suitable for Time-Over-Threshold processing techniques
- requires baseline stabilization at high rates
- linearity an issue
- compensation an issue

Nonlinear pole-zero compensation



- Classical
  - *RF · CF = RC ·CC*
  - *Zero created by RC,CC cancels pole formed by RF, CF*

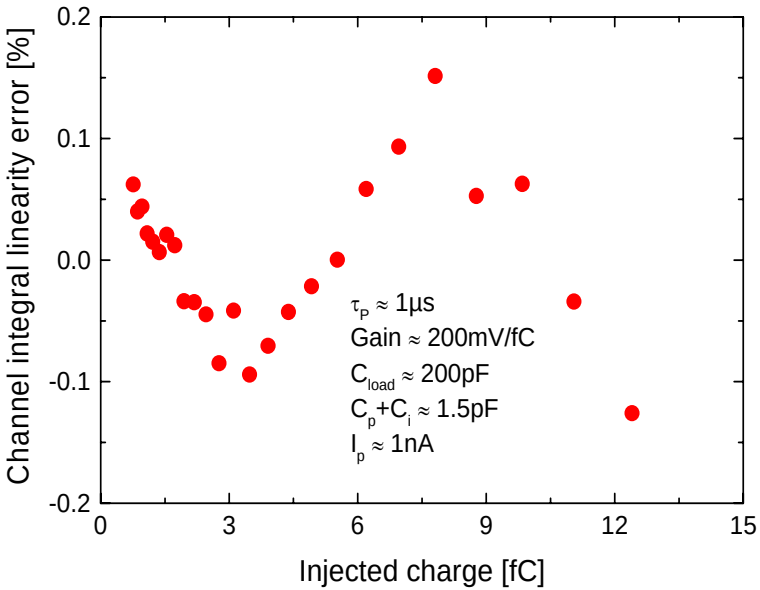


- IC Version
  - *CC = N · CF*
  - *$(W/L)_{MC} = N \cdot (W/L)_{MF}$*
  - *Zero created by MC, CC cancels pole formed by MF, CF*
  - *Rely on good matching characteristics of CMOS FETs and capacitors*

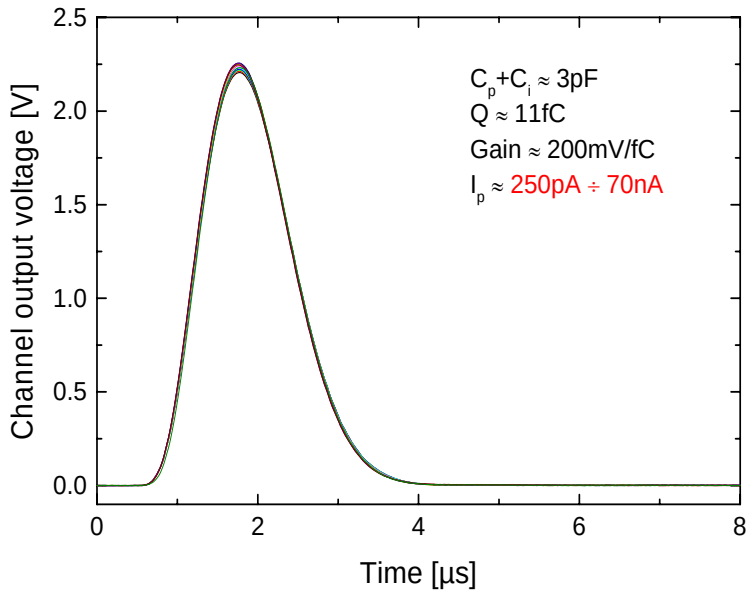
G. Gramegna, P. O'Connor, P. Rehak, S. Hart, "CMOS preamplifier for low-capacitance detectors", NIM-A 390, May 1997, 241 – 250.

Preamp reset with nonlinear PZ compensation – experimental results

linearity



output vs pixel leakage current

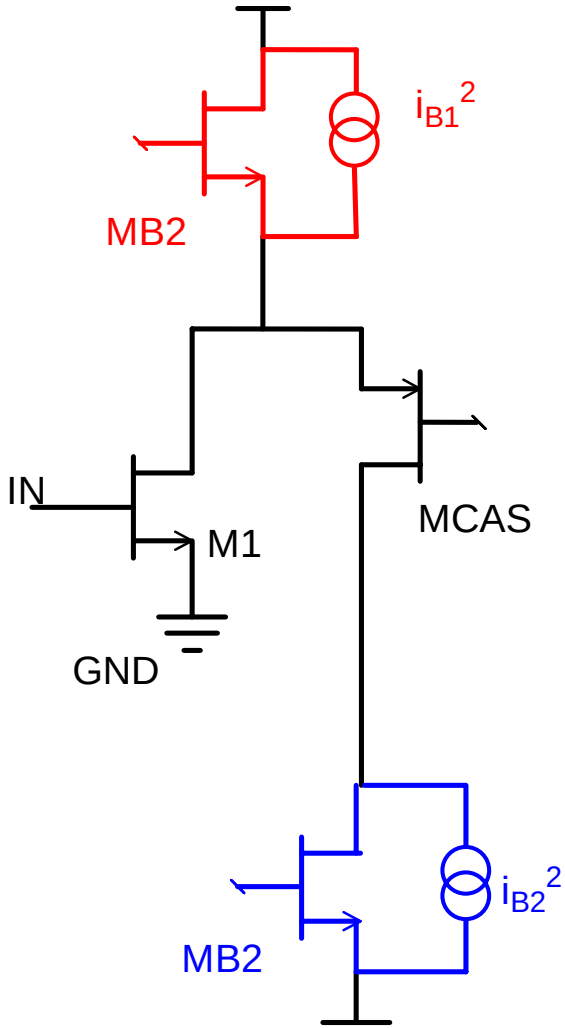


Compensated reset system

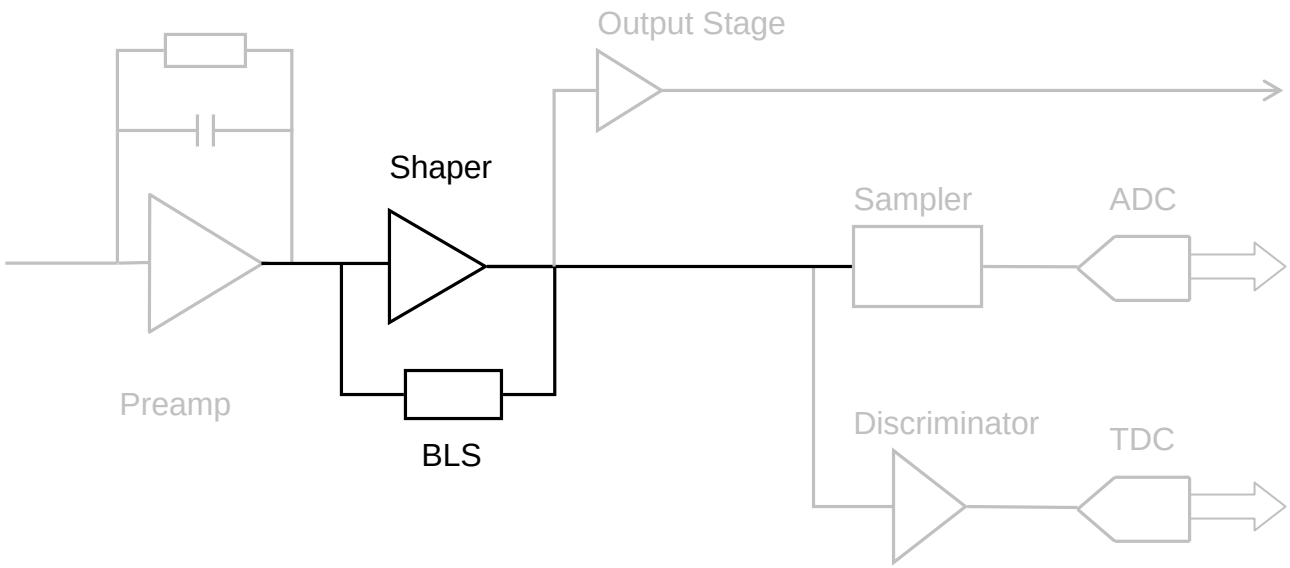
- Advantages:
  - *near theoretical noise contribution*
  - *accepts detector leakage current over wide range*
    - allows DC coupling of detector to preamp
  - *compensate the parasitic preamp feedback pole with a precisely matched zero*
    - allows crude single-element feedback
  - *insensitive to variations in supply voltage, temperature, and process*
  - *internal bias circuit needs no external adjustments*
    - same circuit works for any detector, gain, tp
  - *easy to implement programmable gain*
- Drawbacks:
  - *only works in one polarity*
  - *DC leakage amplified by same factor as signal*
    - requires BLR in 2nd stage
  - *large area consumption*

Secondary noise sources in the preamp

- i_{B1}^2 and i_{B2}^2 are effectively in parallel with the input transistor
- Their contribution to input (white) thermal series noise is $(g_{mB1,2}/g_{m1})^2$.
- We minimize their g_m w.r.t. that of M1
- $g_{mB1,2} = \sqrt{2\mu C_{ox} W I_D / L}$
- use low W/L (i.e. long-gate) devices with large or degenerate with source resistor.
- Keep W/L as small as possible (thus V_{gs}-V_T large) while keeping $V_{DS} > V_{gs}$-V_T.
- Various ways to optimize.



Shaper and baseline stabilizer

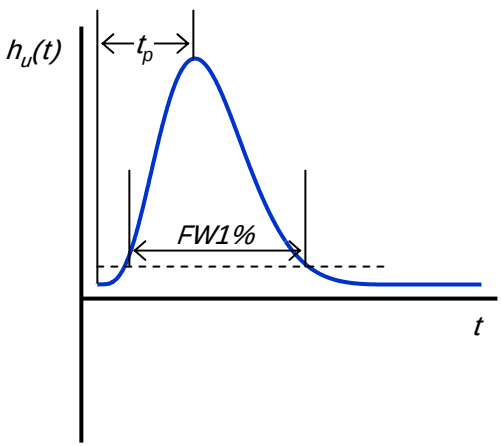


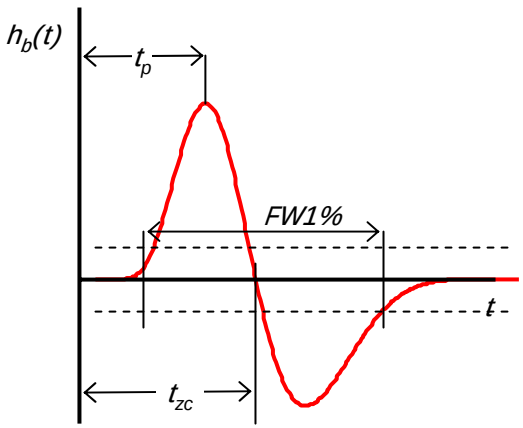
Integrated shaping amplifiers

- Limits the bandwidth for noise
- Gives controlled pulse shape appropriate for rate
- Control baseline fluctuations
- Set slope at threshold crossing for timing
- Bring charge-to-voltage gain to its final value
- By its saturation characteristics, sets upper limit on Q_{in}

- Feedback circuits give the most stable and precise shaping
  - *At the expense of power dissipation*
  - *Poor tolerance of passives limits accuracy of the poles and zeros*
- High-order shapers give the lowest noise for a given pulse width

Shaper Characteristics





first and second moments

$$\int_{-\infty}^{\infty} |h(t)|^2 \, dt$$

$$\int_{-\infty}^{\infty} |h'(t)|^2 \, dt$$

slope at threshold crossing

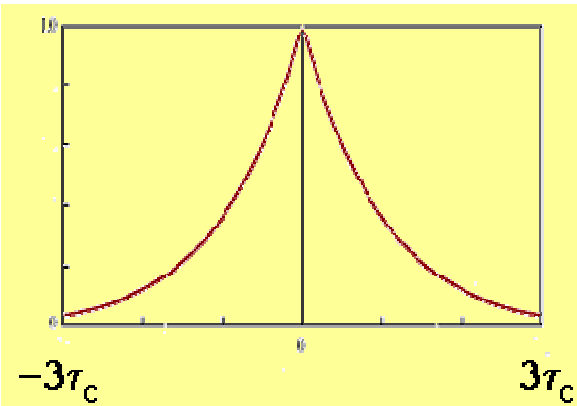
$$h'(t_{TC})$$

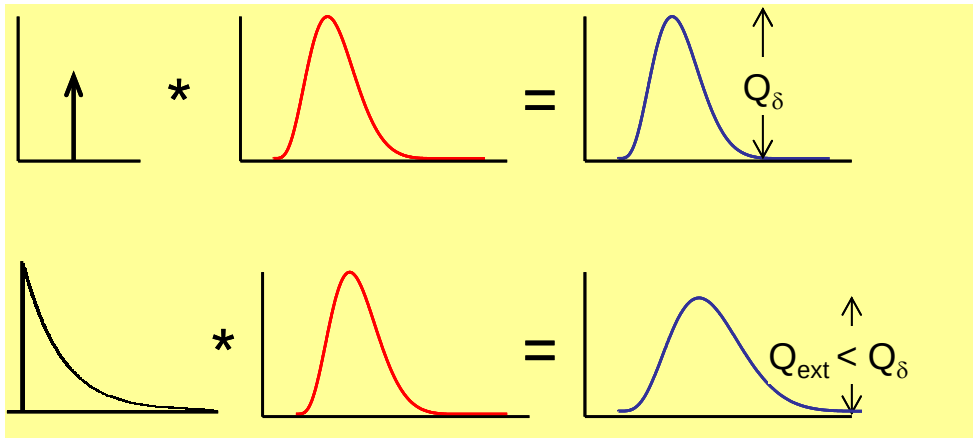
where $h(t_{TC}) = V_{th}$

Pulse shaper – matched filter with compromises

- calculation of matched filter
  - *incomplete knowledge of noise spectrum*
  - *incomplete knowledge of input waveform*
- exact transfer function difficult to realize in practice
- optimum filter requires a long time to respond
  - *pileup ⇔ limited rate capability*
- "ballistic deficit"
  - *input charge is not a δ-function*
  - *width of impulse response must be >> duration of input charge waveform*

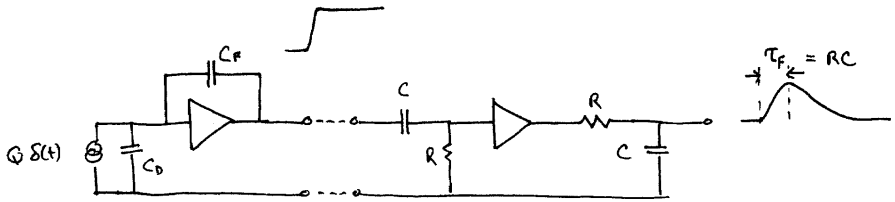
constraints:
- noise corner
- rate^{-1}
- charge collection
- preamp decay





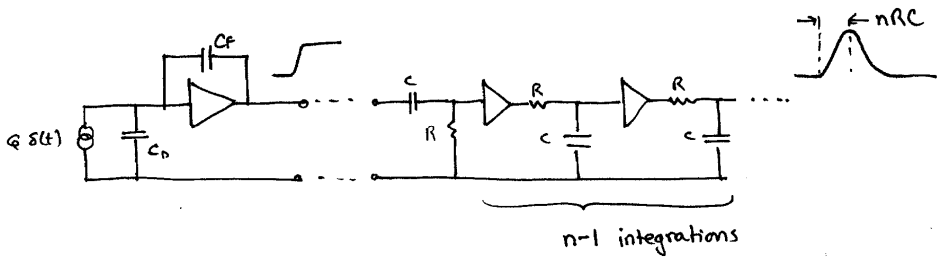
Pulse shaping filters with real poles

Simplest filter: CR-RC

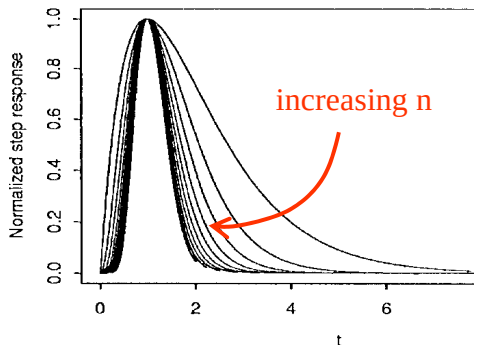


- asymmetric response

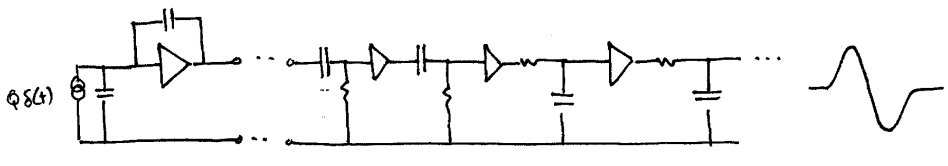
CR-RC^n, unipolar semiGaussian



- Identical real poles
- Symmetry improves with order n:



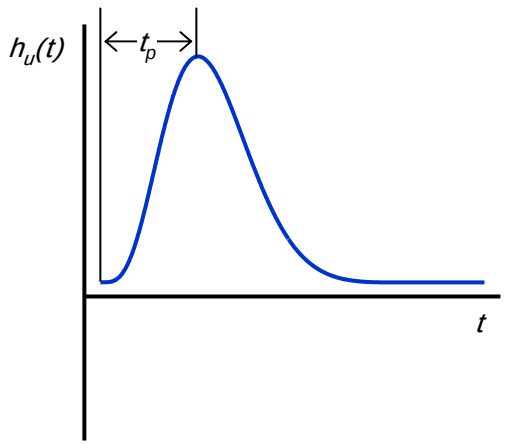
CR^2-RC^n, bipolar semiGaussian



- Area-balanced
- Derivative of CR-RC^n

Properties of real-pole semiGaussian shapers

unipolar CR-RC^n

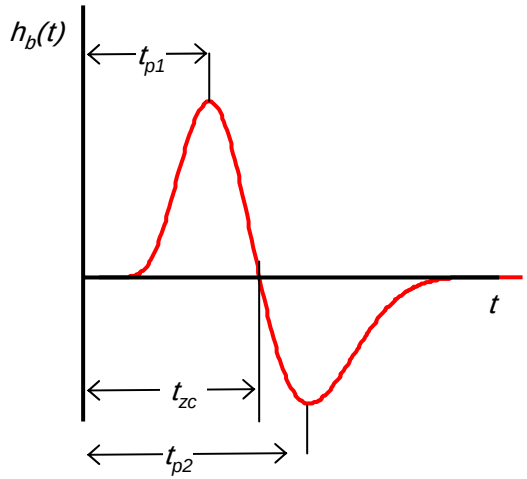


$$H_u(s) = \frac{s\tau}{(1+s\tau)^{n+1}}$$

$$h_u(t) = \frac{1}{n!}\left(\frac{t}{\tau}\right)^n \mathrm{e}^{-t/\tau}$$

$$t_p = n\tau$$

bipolar CR^2-RC^n



$$H(s) = \frac{(s\tau)^2}{(1+s\tau)^{n+2}} \qquad \omega_{\max} = \frac{2}{n\tau}$$

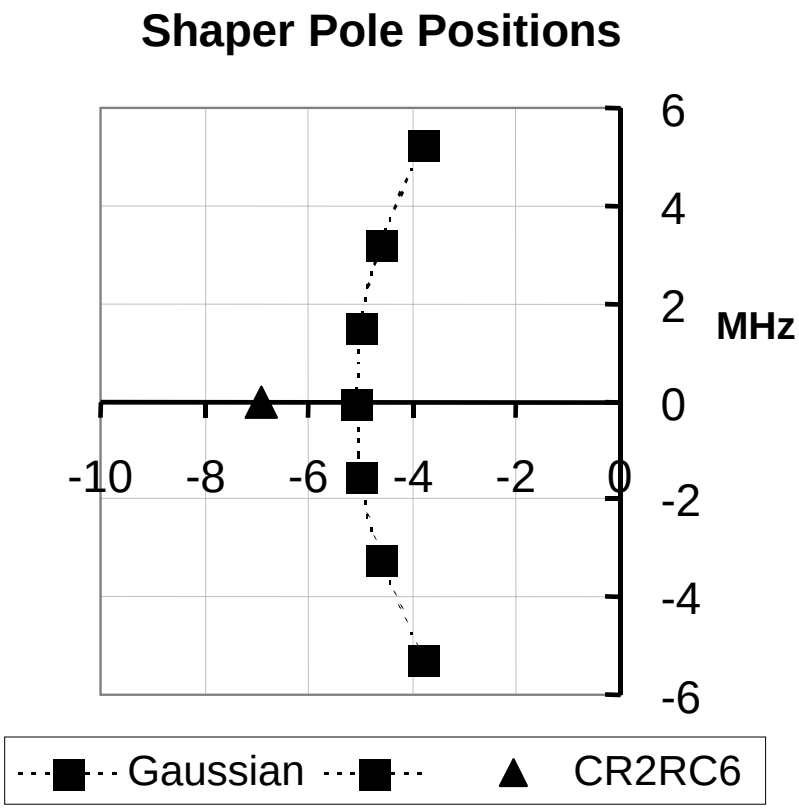
$$h(t) = \frac{1}{(n+1)!\tau}\left(\frac{t}{\tau}\right)^n \mathrm{e}^{-t/\tau}\left[t-(n+1)\tau\right]$$

$$t_{p1} = (n+1-\sqrt{n+1})\tau$$

$$t_{zc} = (n+1)\tau$$

$$t_{p2} = (n+1+\sqrt{n+1})\tau$$

Complex pole approximation to Gaussian pulse



Ohkawa synthesis method (Ohkawa, NIM 138 (1976) 85-92, "Direct Syntheses of the Gaussian Filter for Nuclear Pulse Amplifiers")

For given filter order, gives closest approx. to a true Gaussian

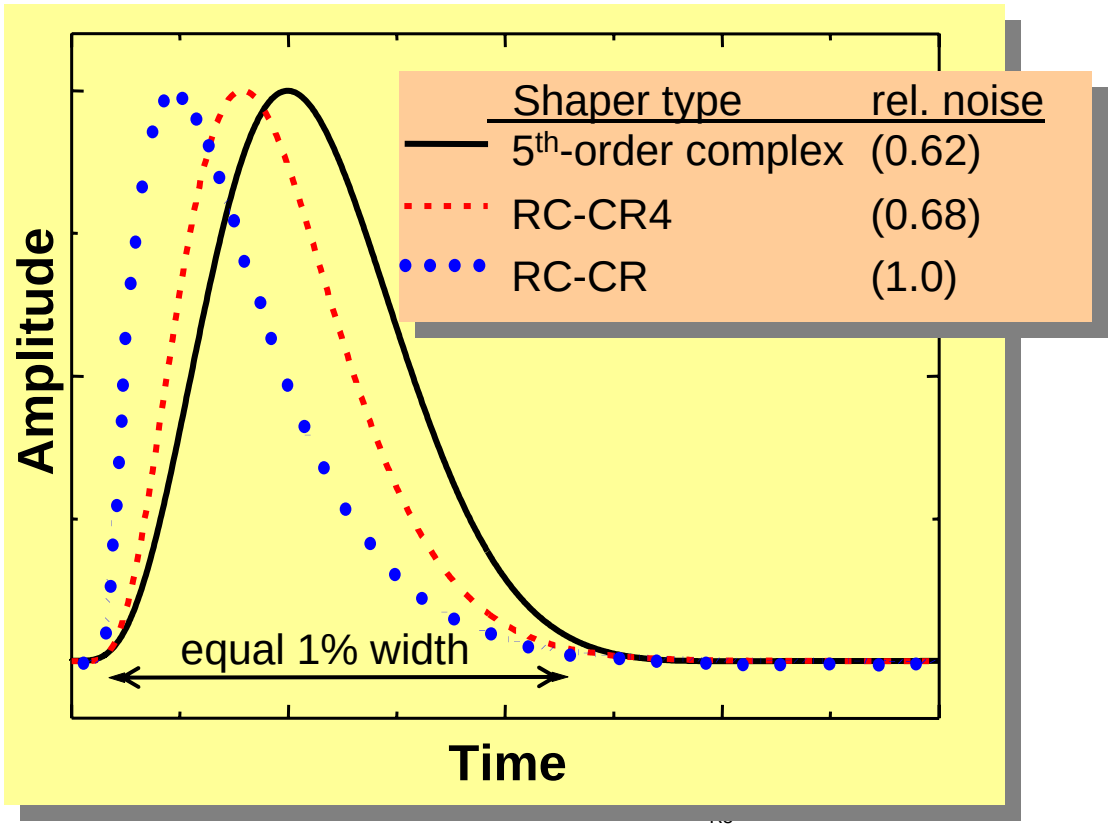
More symmetrical than CR-RC^n filter of same order for same peaking time

Noise weighting functions:

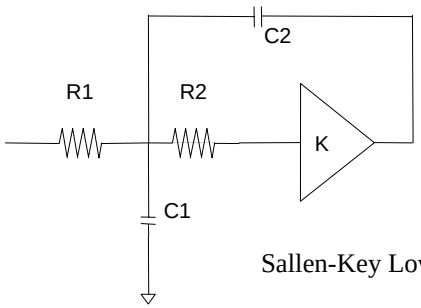
$I_{1,complex}/I_{1,CR\text{-}RC} = 1.18$ series

$I_{2,complex}/I_{2,CR\text{-}RC} = 0.81$ parallel

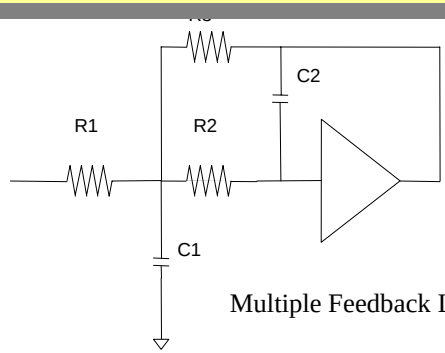
Shaper optimization



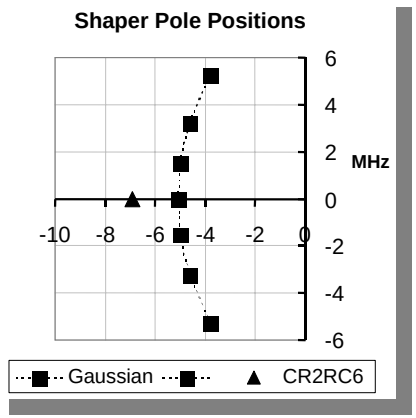
- For a given rate-handling capability, high-order shapers have lower noise.
- Adding an extra shaper stage can reduce noise more than putting the equivalent amount of power into the preamp.
- For a given shaper order, complex pole constellation using second- or third-order active filter topologies minimizes noise.



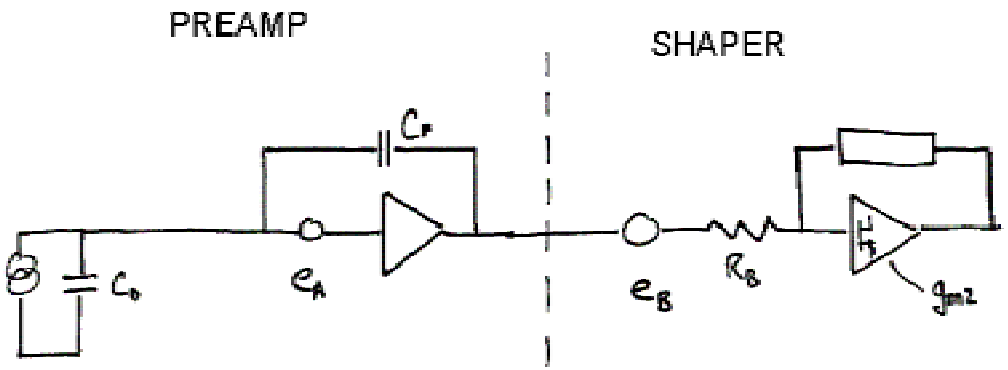
Sallen-Key Lowpass



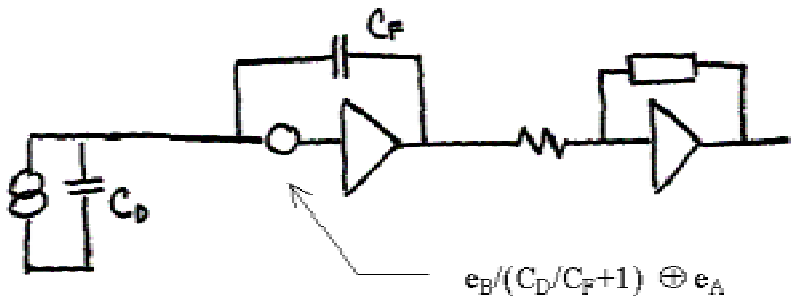
Multiple Feedback Lowpass



Second-stage noise



Transform e_B to the input:



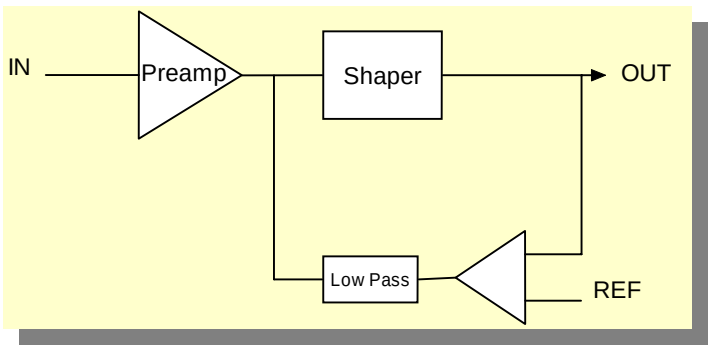
$$\frac{ENC_B}{ENC_A} = \frac{C_F}{C_D} \cdot \left(\frac{R_B}{R_A}\right)^{1/2}$$

Baseline stabilization

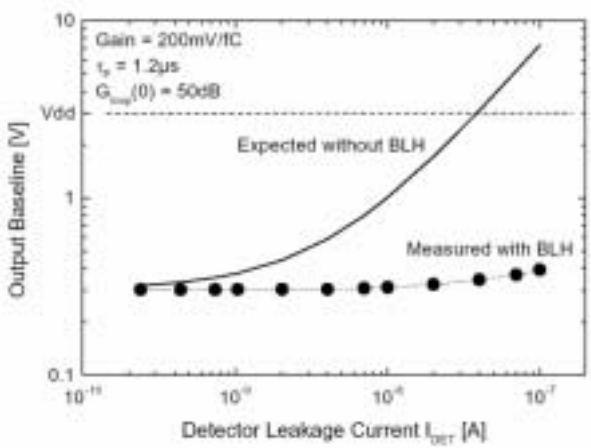
Baseline can move due to:

1. DC coupling to detector with variable leakage
2. Temperature and power supply drift
3. Rate fluctuations in a system with AC coupling

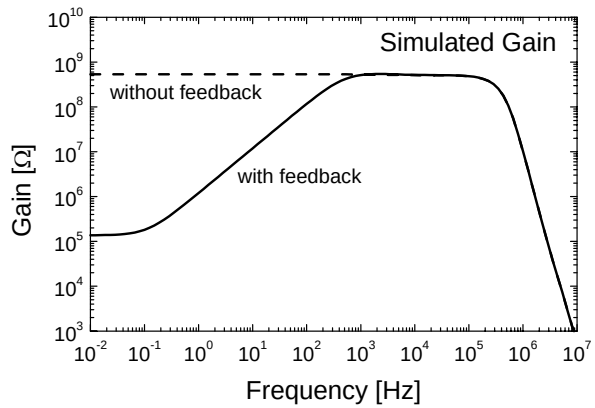
(1) and (2) can be prevented by low frequency feedback circuit:



Result:



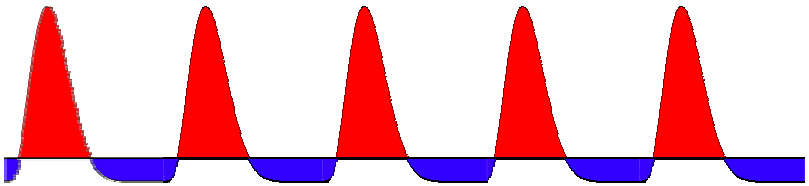
But this introduces unintended AC coupling:



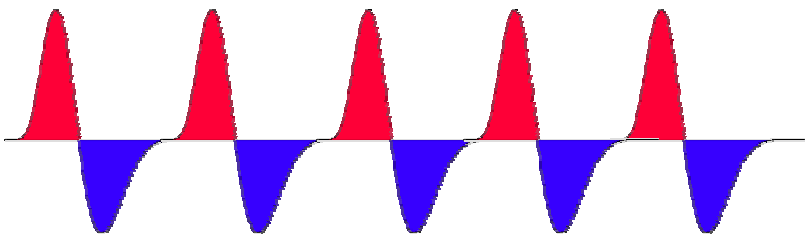
Compensate with nonlinear element or gating of the feedback circuit

Area balance after AC coupling

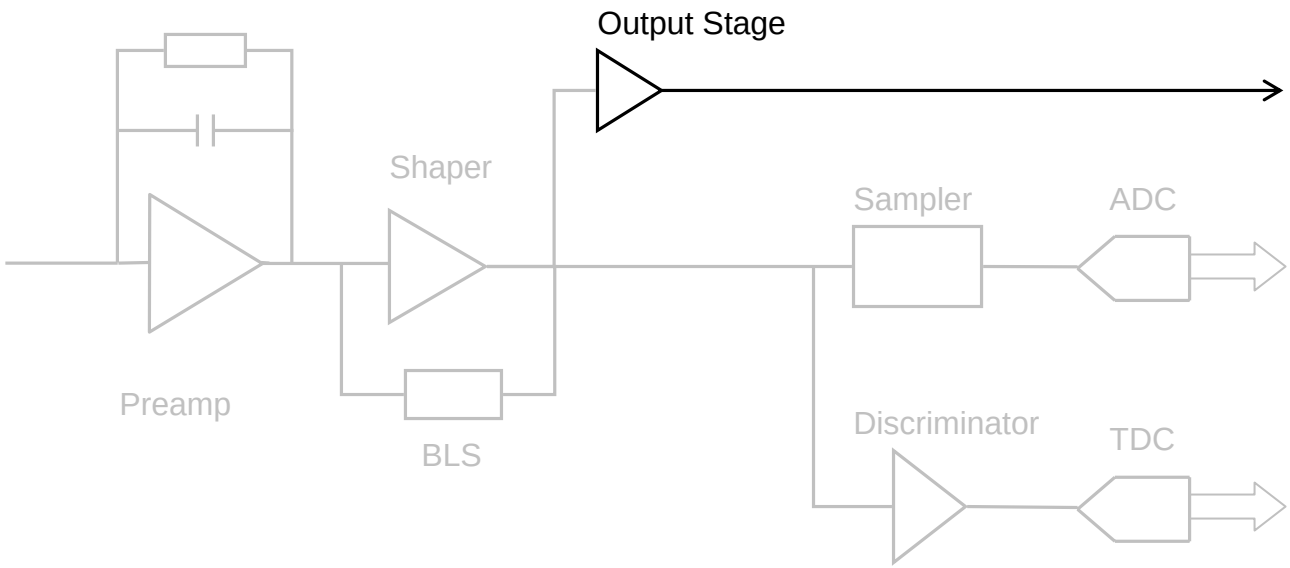
- Unipolar pulse:
- baseline displaced below 0
- instantaneous rate fluctuations cause baseline to wander



- Bipolar pulse:
- each pulse is area balanced, no detrimental effect of AC coupling
- penalty is higher noise, longer occupancy per pulse

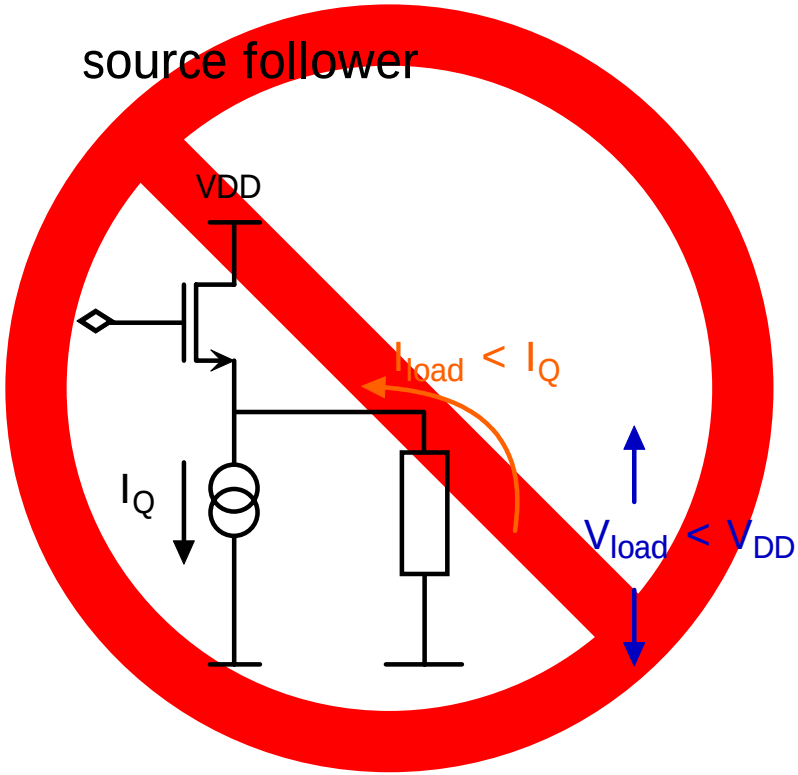


Output stage



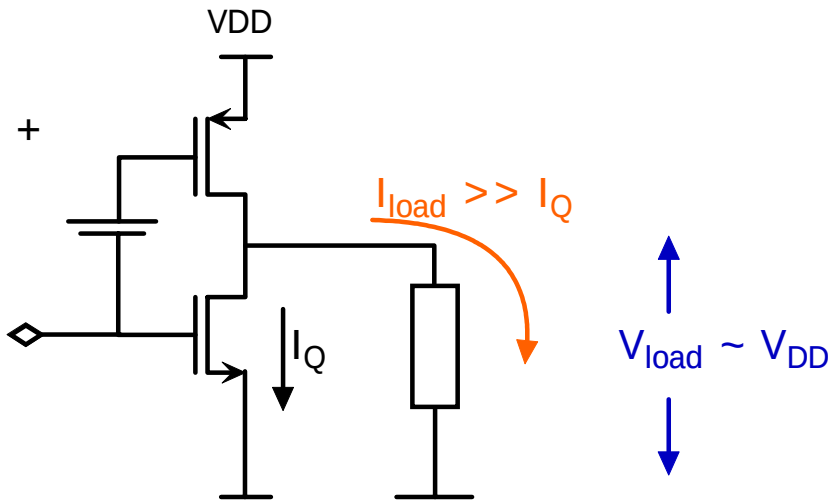
Output driver

source follower



- class A: high standing current
- can't swing rail-to-rail

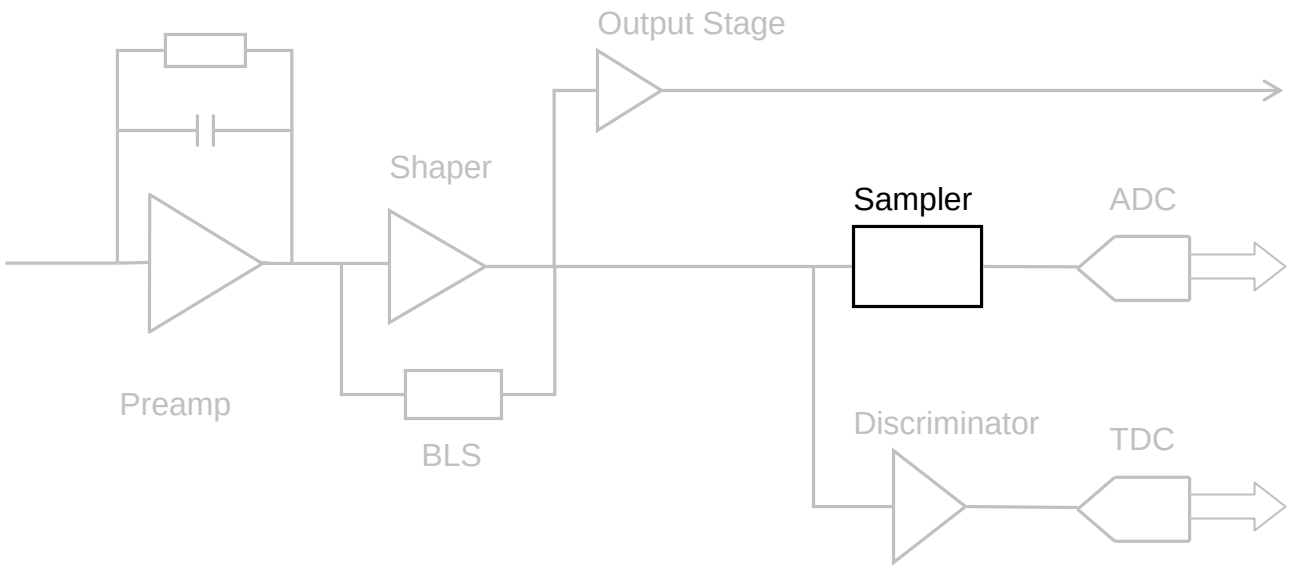
class AB common source



- class AB stage can source or sink currents >> quiescent current
- common-source stage can drive rail-to-rail

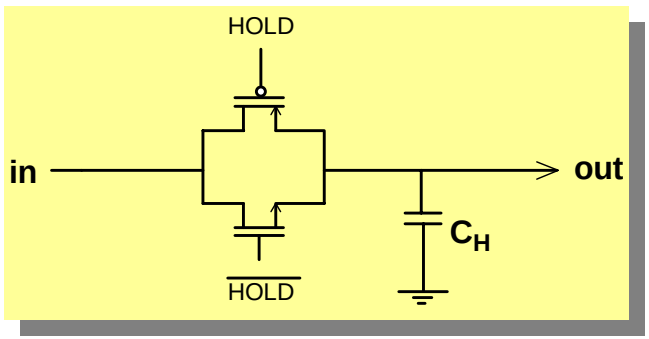
Hogervorst ref.

Analog sampling



Candidate sampling/memory cells in CMOS

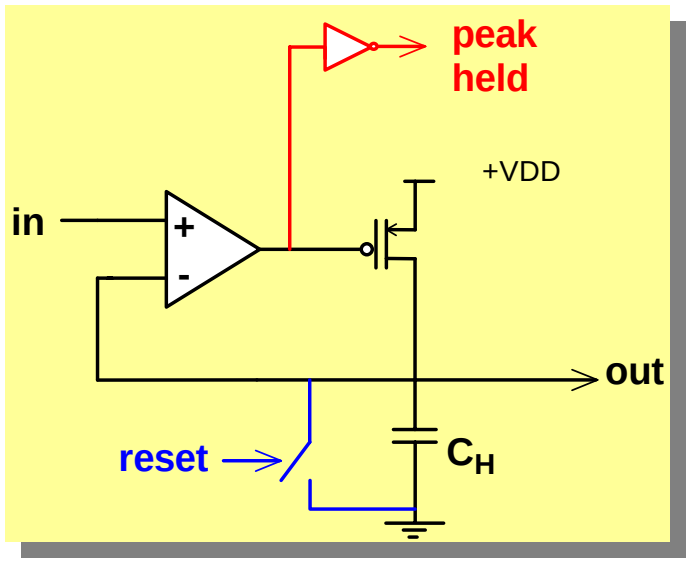
Sample/hold using switched capacitor



- small
- low-power

- timing of hold signal: needs CFD for walk-free operation
- switch charge injection
- poor drive capability: needs output amp

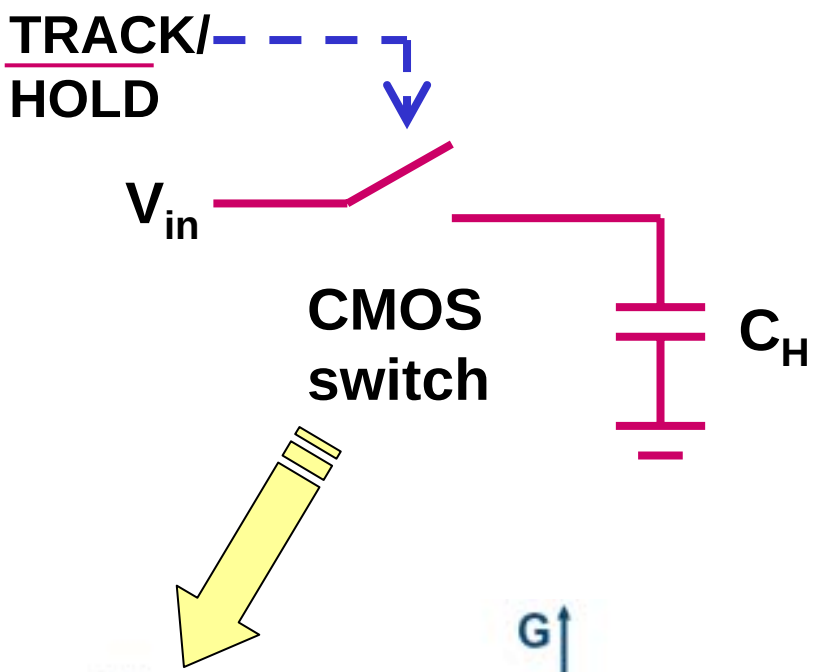
Peak Detector (PD)

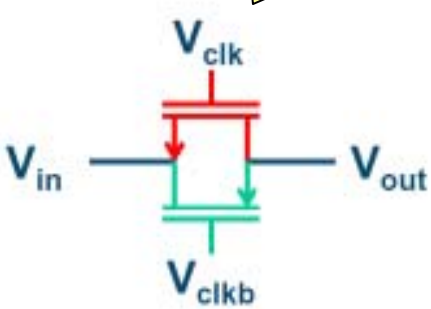


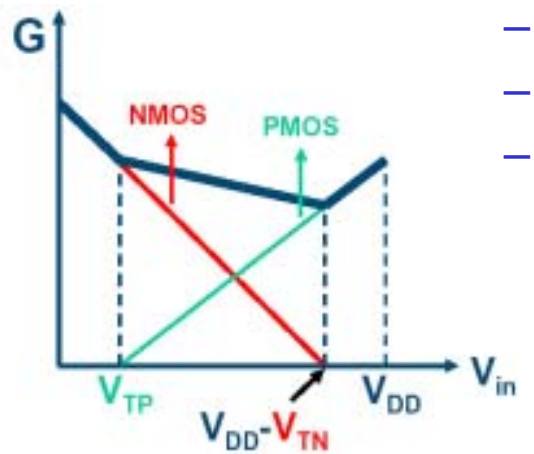
- self-triggered
- timing output
- feedback loop

- deadtime until readout reset
- poor drive capability
- accuracy impaired by opamp offsets, CMRR, slew rate

Switched-capacitor track-and-hold







CMOS switch:

- *low I_{off}*
- *high G_{on}, $0 < V_{sig} < V_{DD}$*

MOS/MIM capacitor:

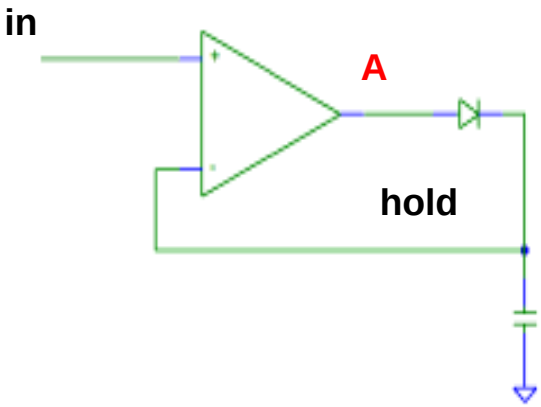
- *well-matched*
- *low leakage*
- *linear*

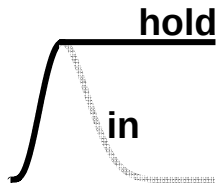
Design tradeoffs:

- *speed – droop rate*
- *speed – charge injection*
- *speed – clock feedthrough*
- *low voltage limits*

CMOS Peak Detector

Classical peak detector





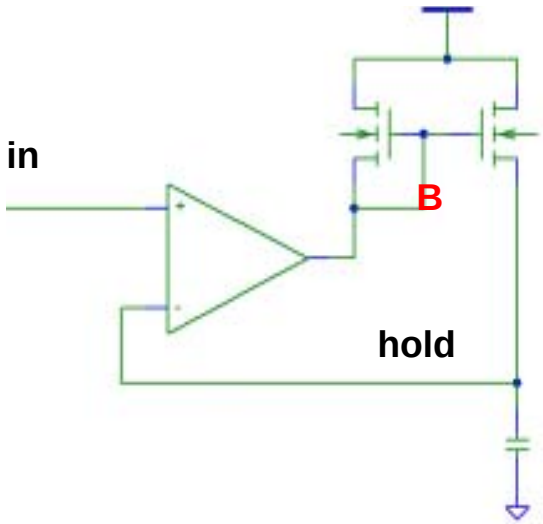
Diode replaced by current mirror acting as rectifying and loop-stabilizing element.

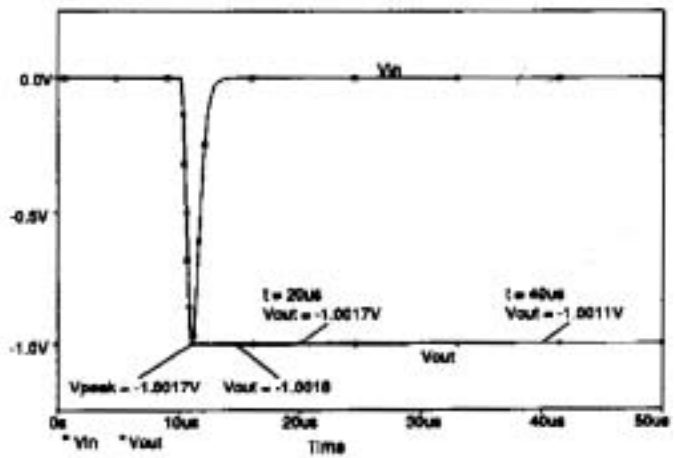
Reduced charge injection from sharp transient at node A(B).

$\Delta V_A = V_P$; $\Delta V_B = V_{th} << V_P$

Accuracy, speed, and dynamic range limited.

Improved CMOS version



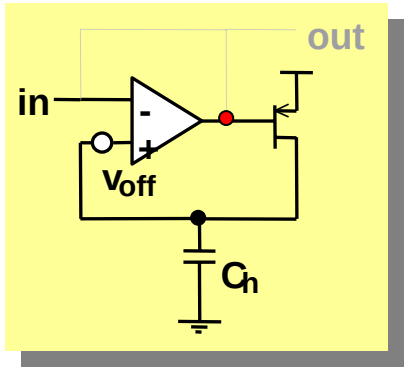


M. W. Kruiskamp, D. M. W. Leenaerts, IEEE Trans. Nuclear Sci., 41(1) 295 (1994)

The two-phase peak detector concept

Write phase

• behaves like classical configuration



Read phase

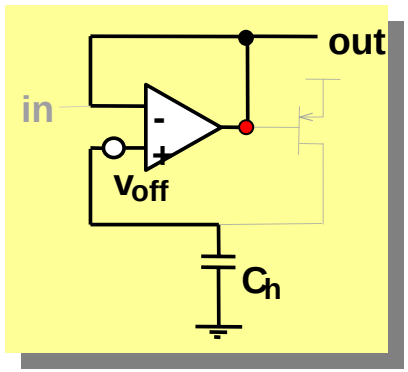
• op-amp re-used as buffer

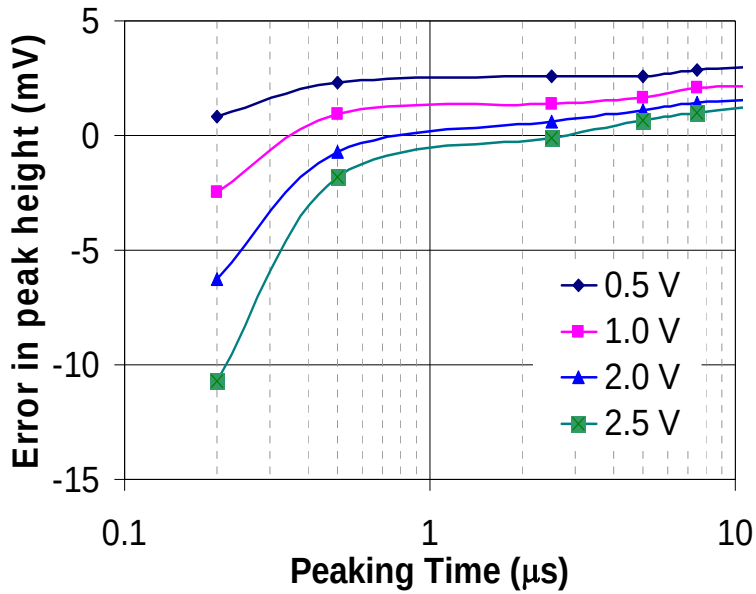
• **offset** and **CMMR** **errors canceled**

• enables **rail-to-rail** sensing

• good **drive capability**

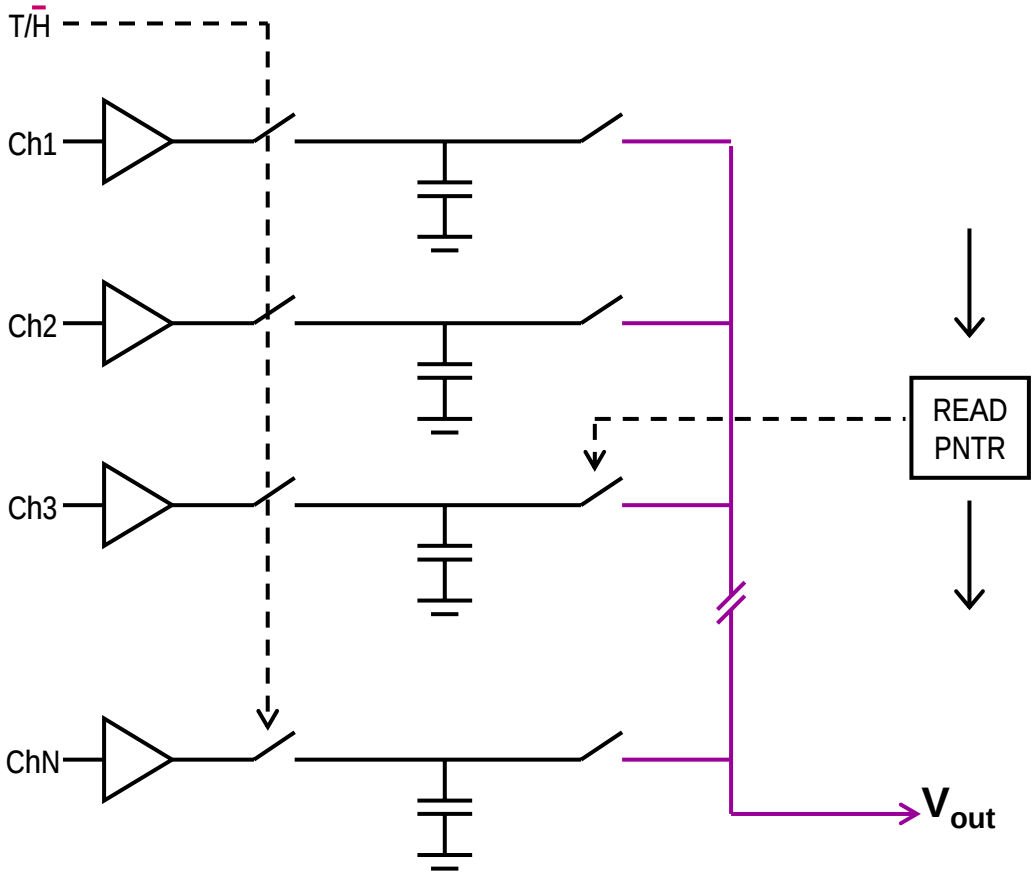
• **self-switching** (peak found)





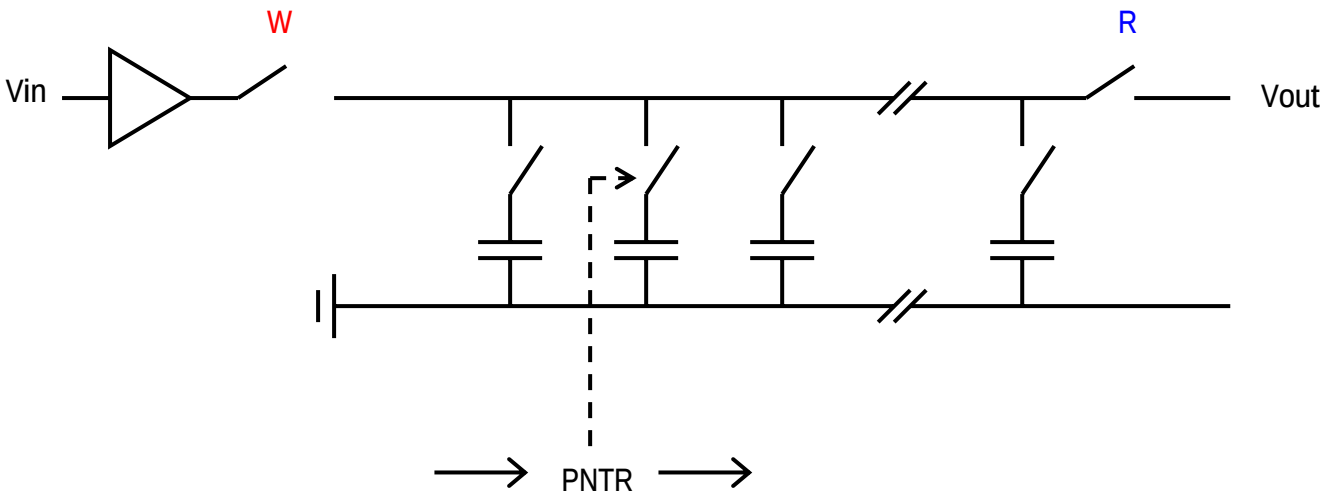
P. O'Connor, G. De Geronimo, A. Kandasamy,, IEEE Trans. Nucl. Sci. 50(4), 892 (2003)
G. De Geronimo, P. O'Connor, A. Kandasamy, Nucl. Instr. Meth. A484, 533 (2002)

Track/hold array + N-to-1 multiplexer

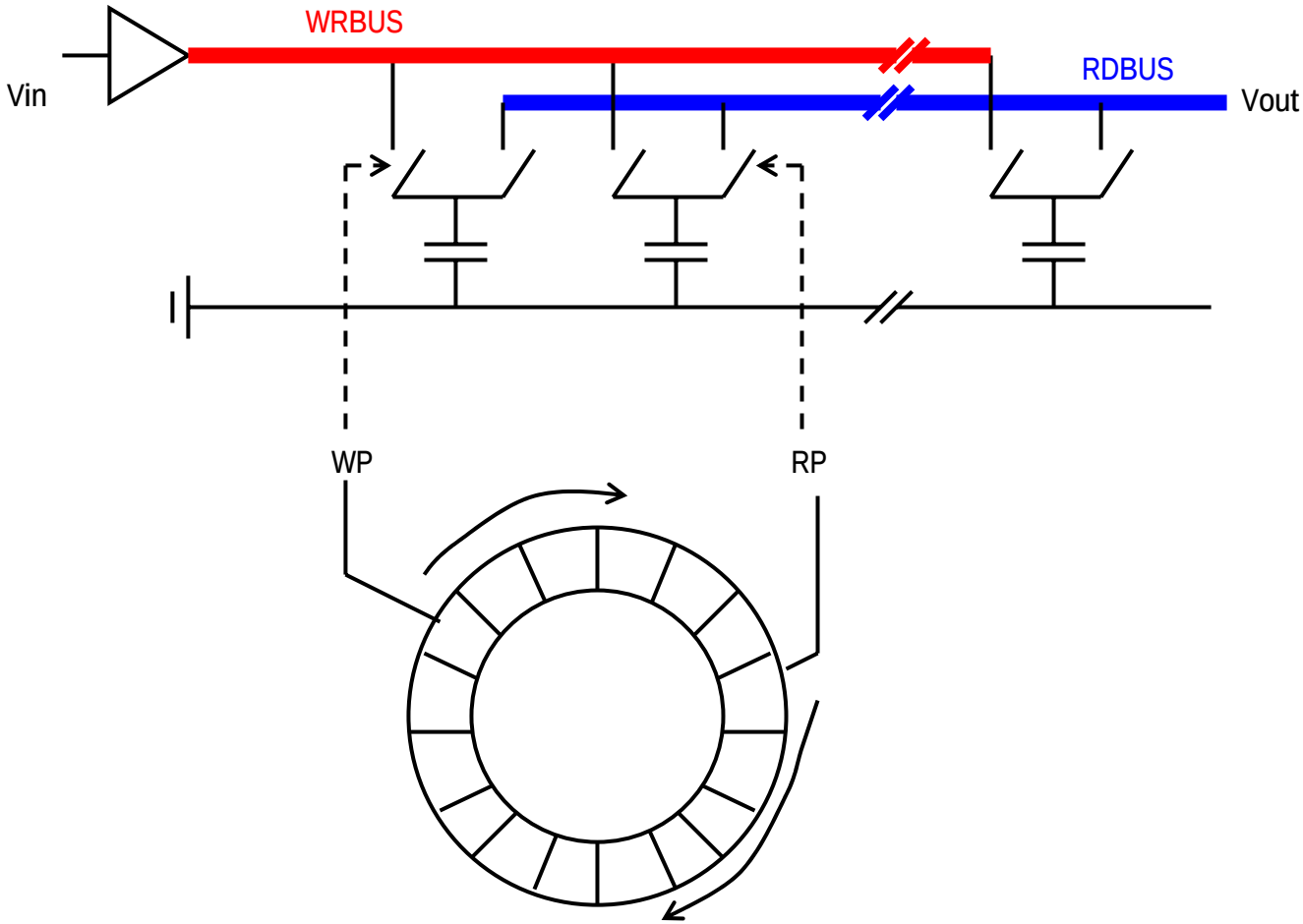


- tradeoff of multiplexing ratio, deadtime
- good channel-channel matching
- requires external signal to control track/hold

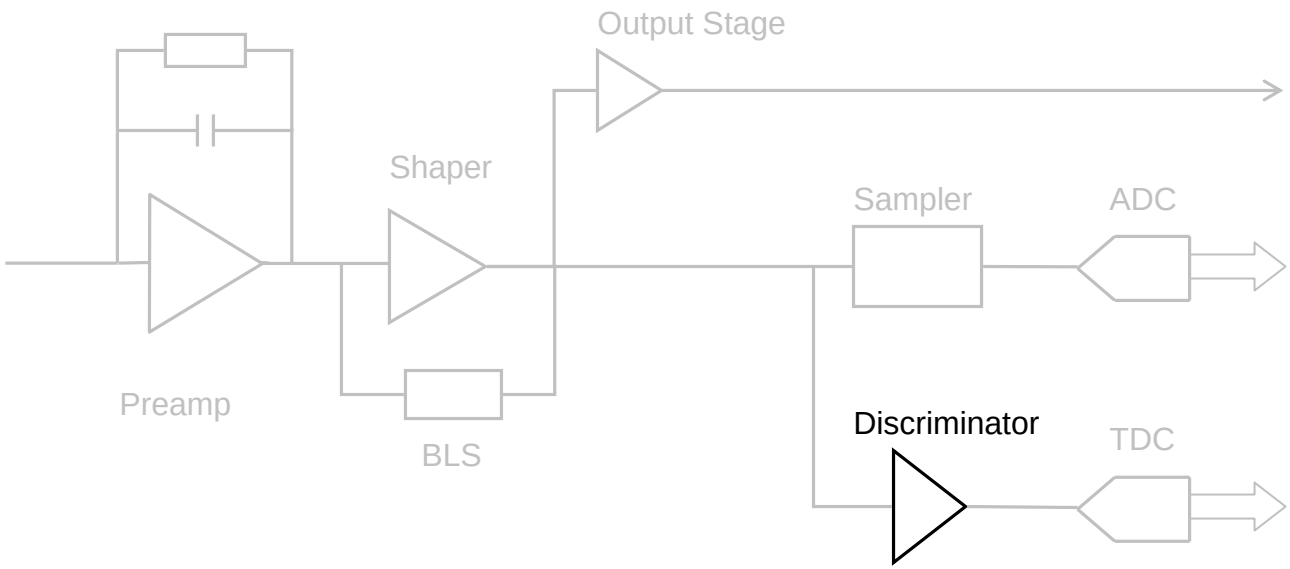
Switched-capacitor array waveform recorder



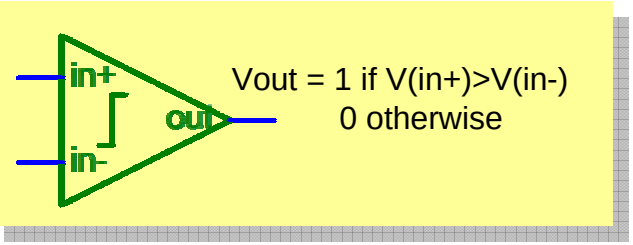
Deadtimeless SCA with simultaneous R/W



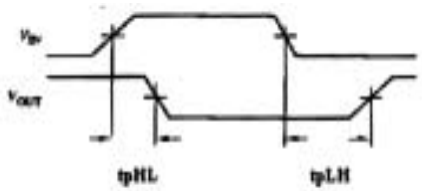
Discriminator

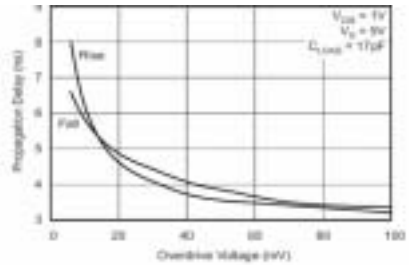


Discriminator properties and applications

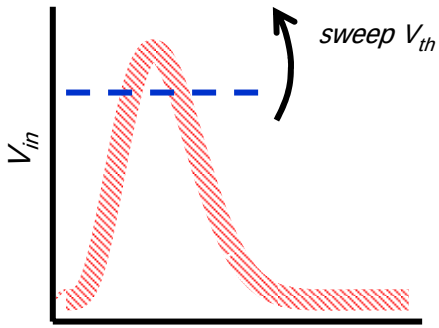


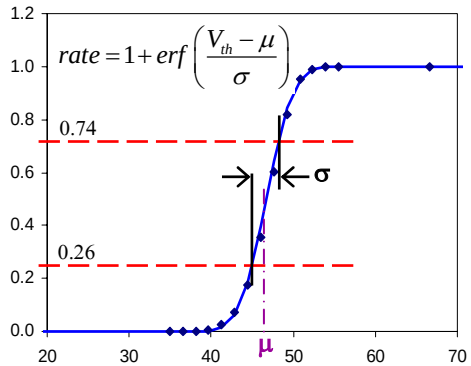
Vout = 1 if V(in+)>V(in-)
0 otherwise





- Characteristics
  - *propagation delay*
    - vs. overdrive
    - vs. risetime (of input wfm)
    - vs. load capacitance
  - *hysteresis*
  - *recovery from saturation*

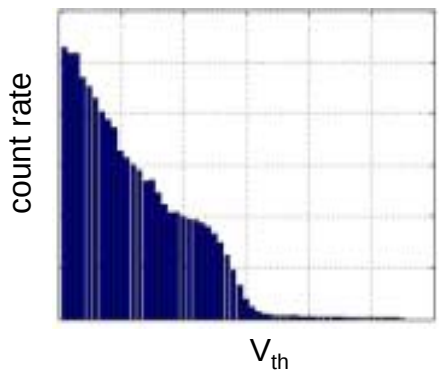


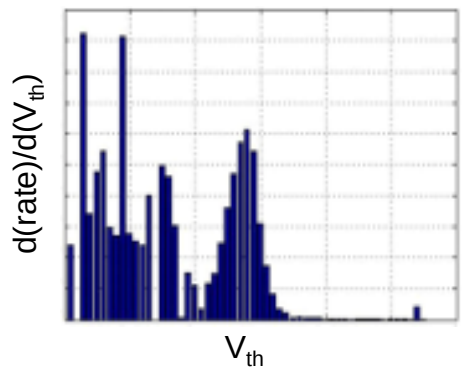


- Used for
  - *hit detection (YES/NO)*
  - *trigger*
  - *amplitude windowing*
  - *amplitude spectra (by threshold sweep)*
  - *time interval marker*

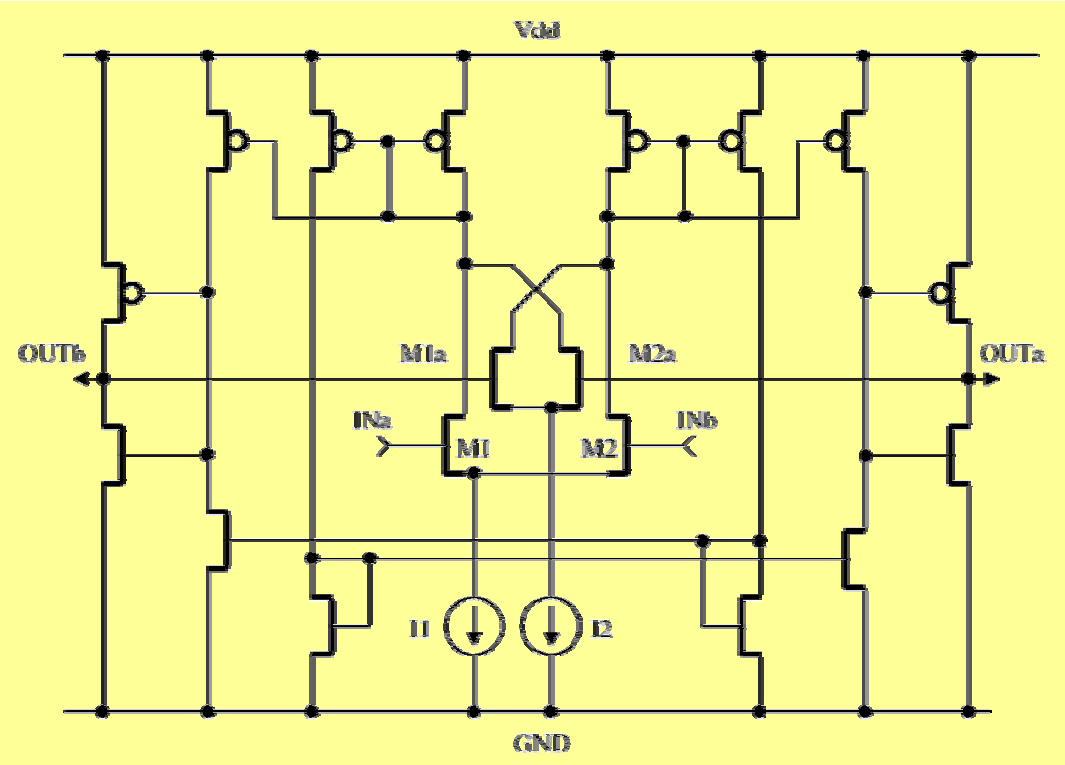
Noise hit rate in threshold detection:
System bandwidth B, rms noise σ ➔

$$f_{noise} \approx 0.6B\exp\left(-\frac{V_{th}^2}{2\sigma^2}\right)$$



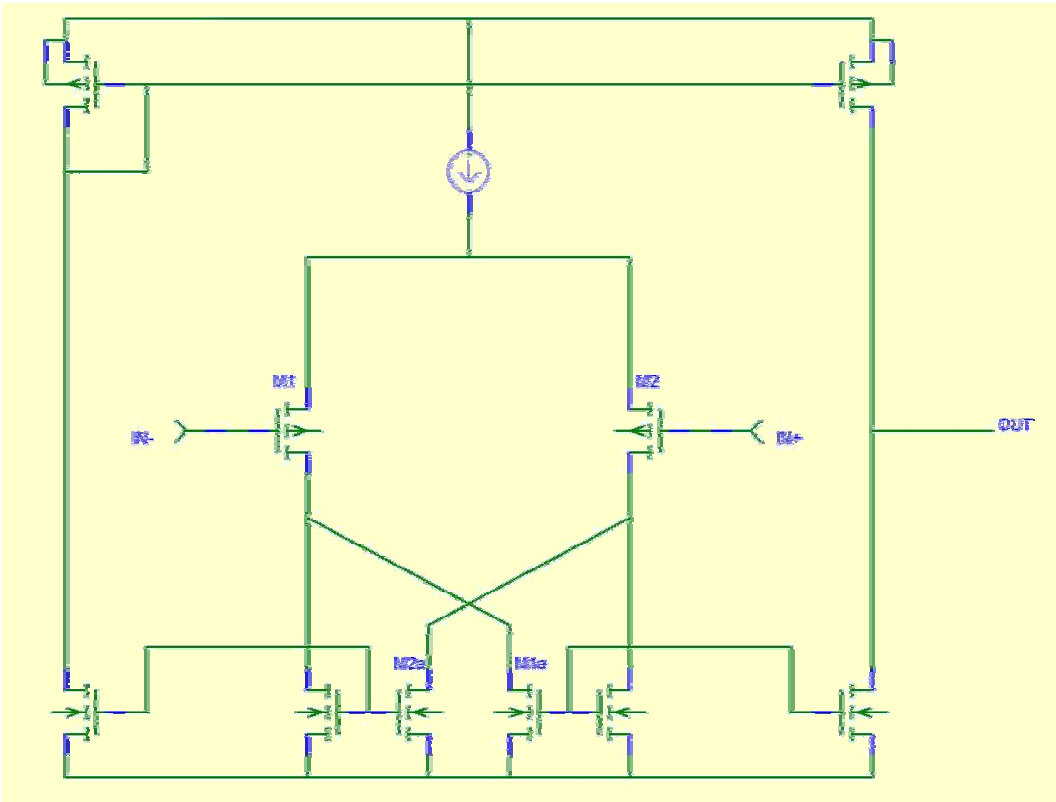


CMOS discriminator topologies (1)



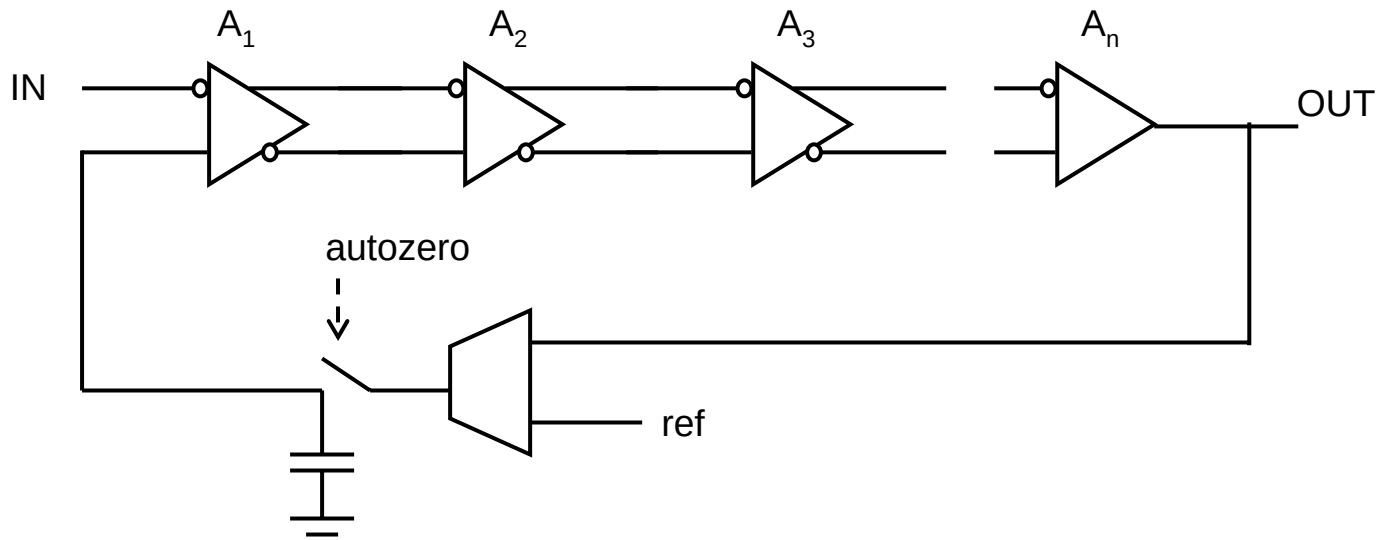
- Main differential pair M1-M2 plus dual current mirrors provide gain ~ 500
- Cross-coupled pair M1a, M2a provide positive feedback.
- Hysteresis level adjustable by I2/I1 ratio.
- Balanced, fully differential circuit less prone to feedback oscillation.

CMOS discriminator topologies (2)

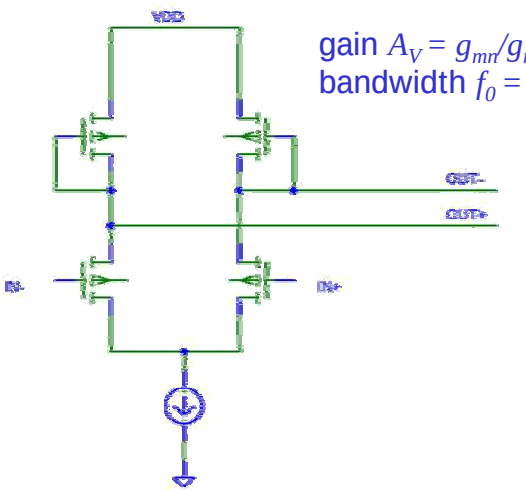


- Cross-coupled pair M1a, M2a provide positive feedback
- Hysteresis level adjustable by M1/M1a width ratio

Cascade topology



gain stage



gain $A_V = g_{mn}/g_{mp}$
bandwidth $f_0 = g_{mp}/2\pi C_{out}$

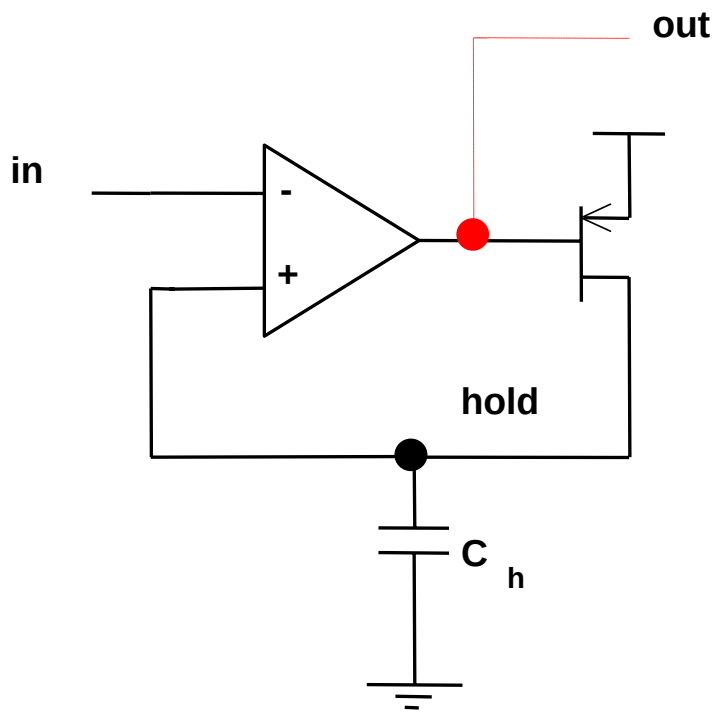
Overall gain A_V^n

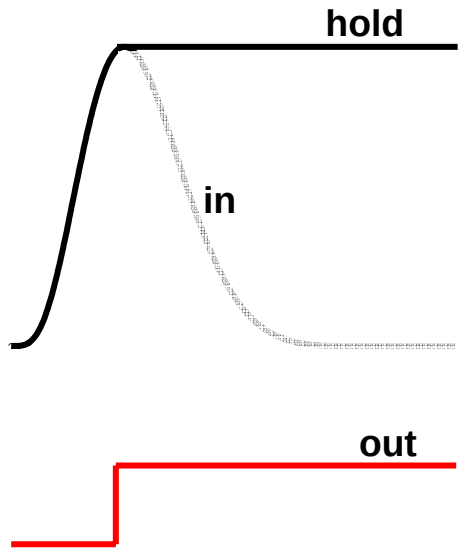
Overall BW $f_0\sqrt{2^{1/n}-1}$

- Cascade gain increases faster than bandwidth decreases as add more stages.
- Nonlinearities limit n to ~ 5 - 6 in practice.

M.L. Simpson et al., IEEE J. Solid-State Circuits 32(2), 1997 (198)
N. Paschalidis et al., IEEE Trans. Nuc. Sci. 49(3), 2002 (1156)

Peak detector as timing comparator

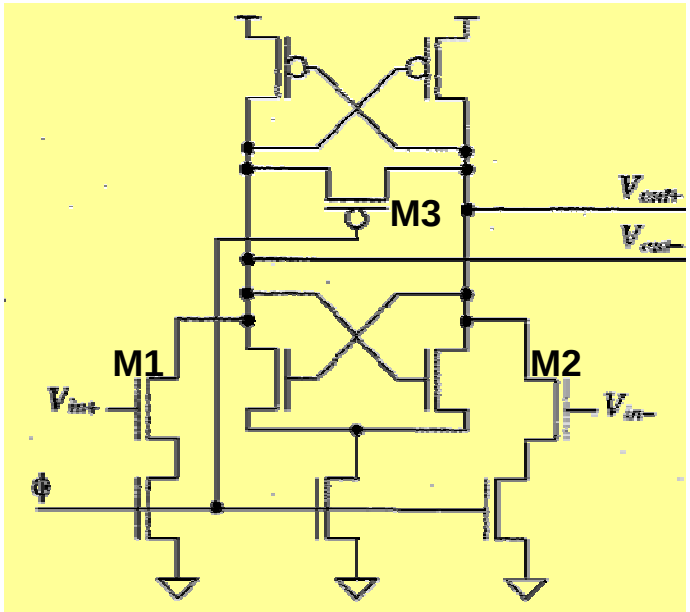




C_h may be precharged to threshold

V_{out} is free of time-walk

Clocked comparator

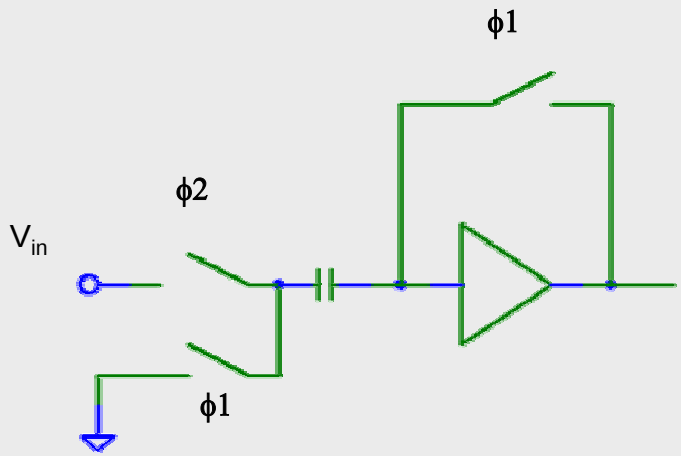


ϕ=0:
M3 holds latches in balanced condition

ϕ=1:
M3 OFF, M1/M2 unbalance latches, positive feedback gives rapid response

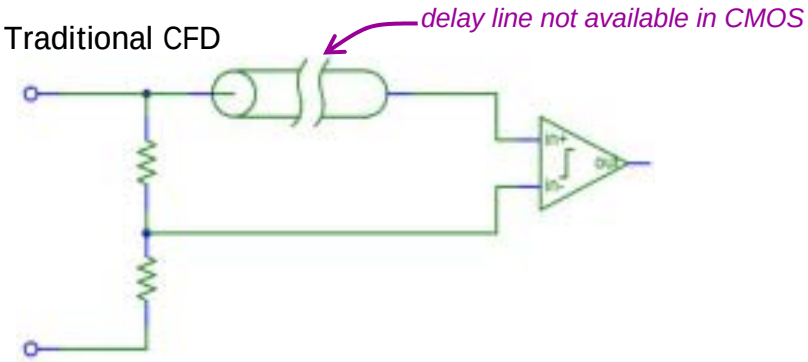
• This topology frequently used in ADCs.

Comparator offset cancellation by autozeroing

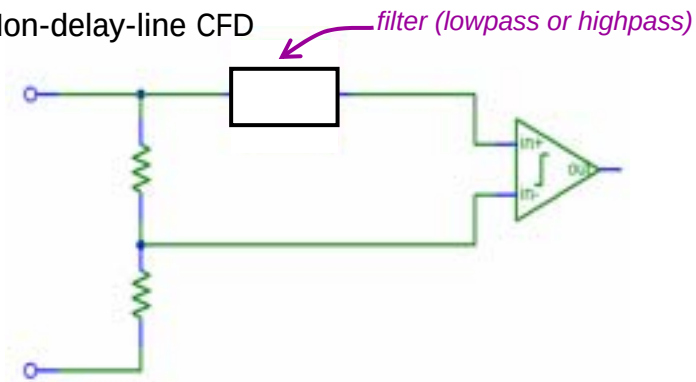


Non-delay-line constant fraction discriminators

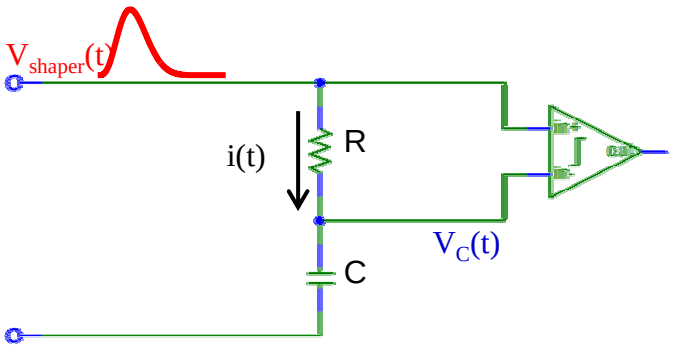
Traditional CFD

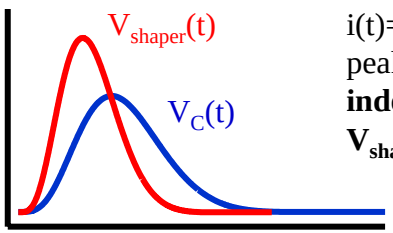


Non-delay-line CFD



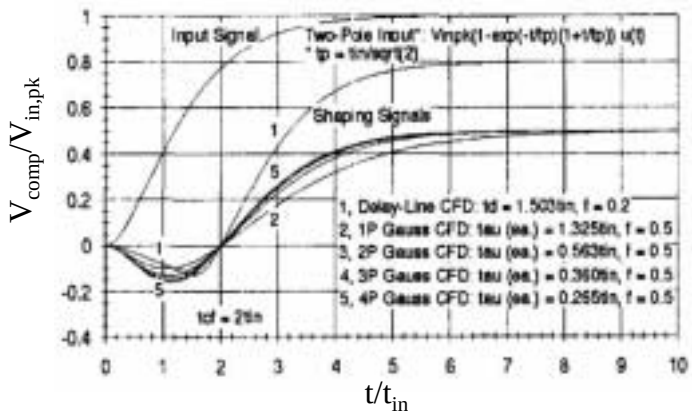
Simple monolithic implementation





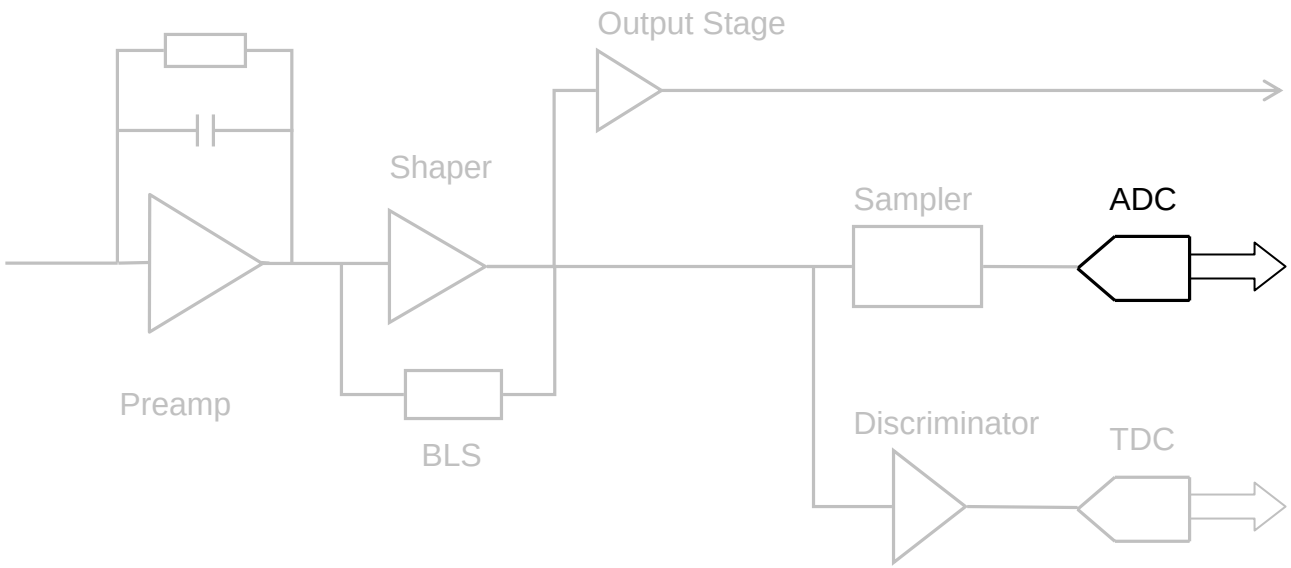
i(t)=0 when $dV_C(t)/dt=0$, i.e. at peak of lowpass waveform **independent of amplitude of $V_{shaper}(t)$**

Higher-order filter improves slope at zero-cross and leading-edge sensitivity

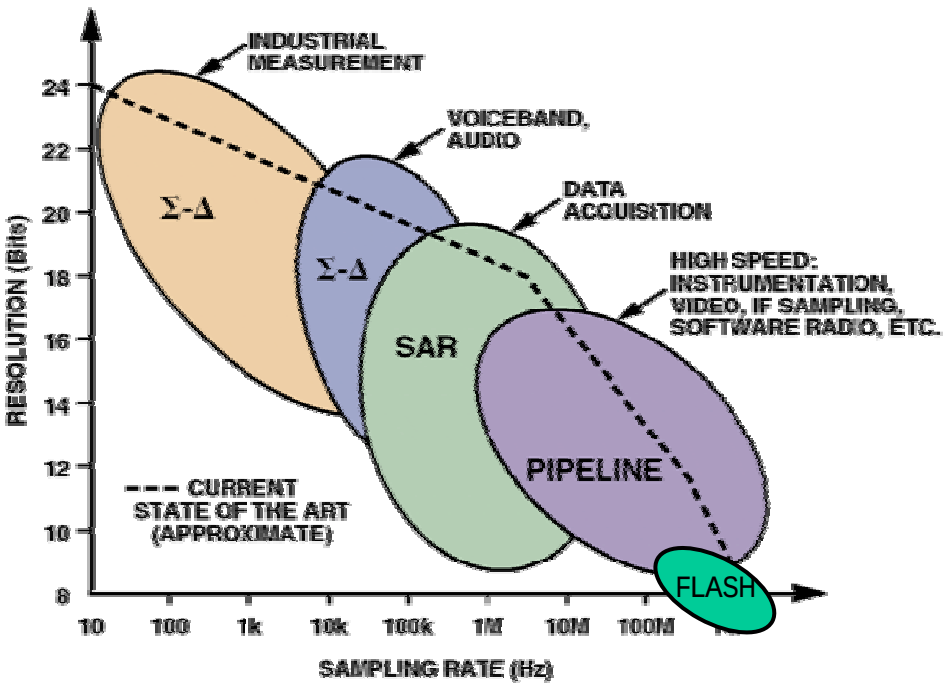


B.T. Turko, R.C. Smith, IEEE Trans. Nuc. Sci. 39(5), 1992 (1311)
C.H. Nowlin, Rev. Sci. Instr. 63(4), 1992 (2322)
D.M. Binkley, IEEE Trans. Nuc. Sci. 41(4), 1994 (1169)

Analog-to-digital converter (ADC)



ADC architectures

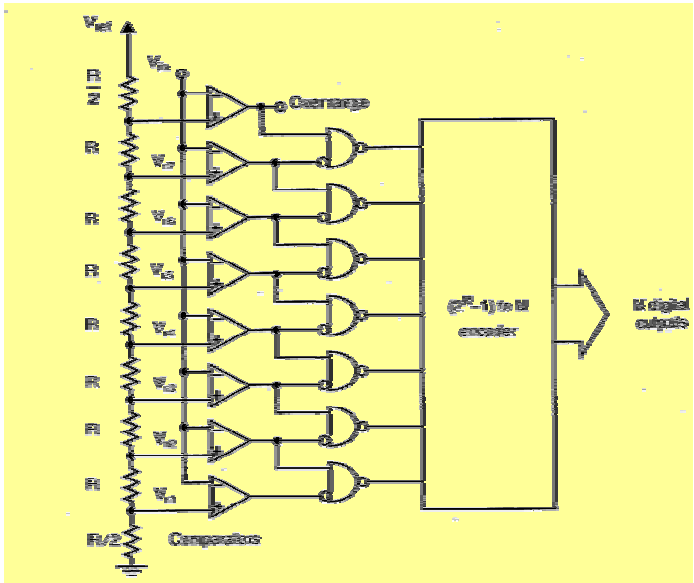


Tradeoffs:

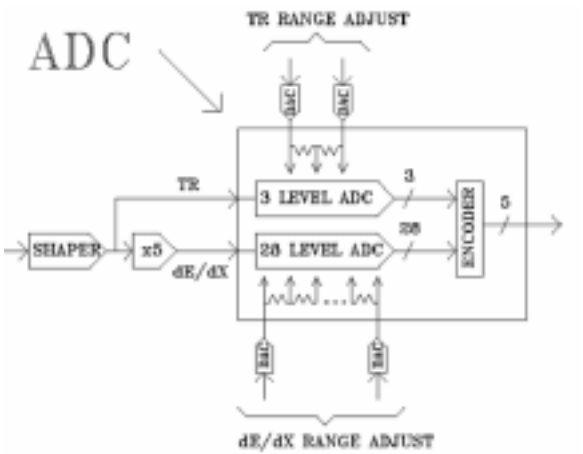
- speed
- power
- resolution

W. Kester, Analog Dialogue 39(2), 2005 (11)

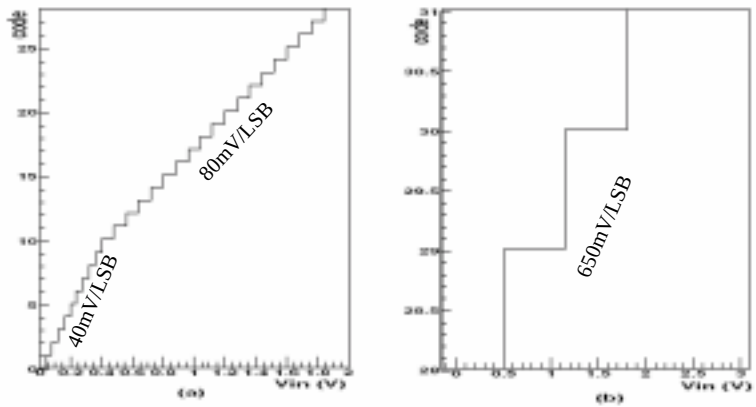
Flash converter



- N-bit converter requires 2^N-1 comparators and resistors
- Converts in one clock cycle (no latency)
- Comparator offset must be < $V_{FS}/(2^N)$
- Vin must be able to drive large dynamic load of comparator array
- Resistor string may be tapped for piecewise-linear transfer function

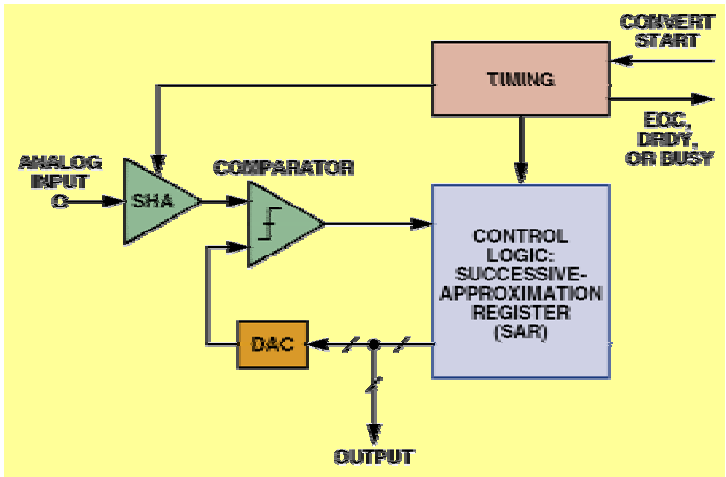


5 bit output
9 bit dynamic range



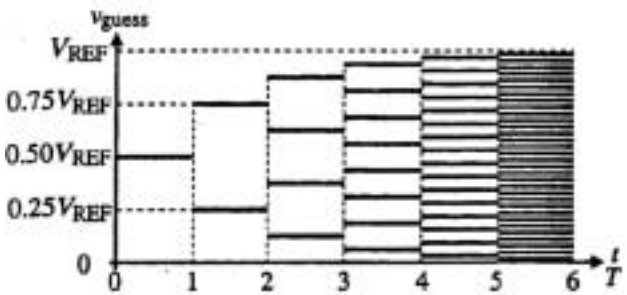
K. Barish et al., Nuclear Science Symposium Conference Digest IEEE, Nov. 2001, 604

Successive Approximation (SAR) converter

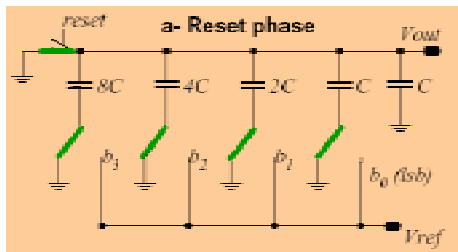


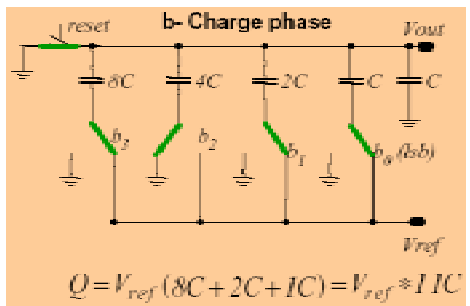
- Performs binary search using N-bit accurate DAC
- Charge-redistribution DAC gives 10 bit accuracy without calibration for typical 0.1% capacitor matching
- With digital autocalibration accuracy improves to 18-bit
- N-bit conversion requires N comparisons
- Sample-and-hold required at input so value to be converted does not change during the conversion time

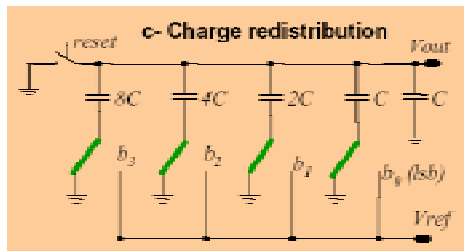
Binary search



Charge Redistribution DAC Example: 4Bit DAC- Input Code 1011





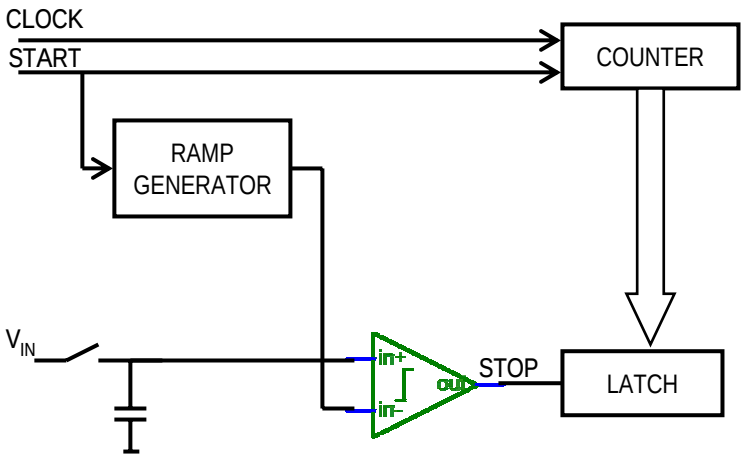


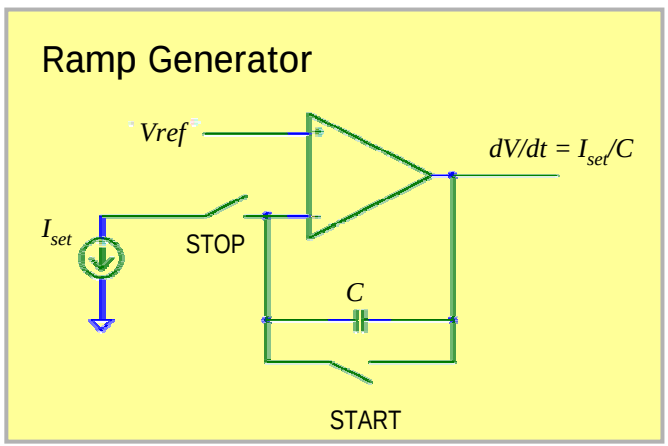
$$V_{ref} * 11C = V_{out} * 16C$$

$$\rightarrow V_{out} = \frac{11}{16} V_{ref}$$

In SAR converter, CDAC also combines functions of sample/hold and subtractor

Single-slope (Wilkinson) integrator

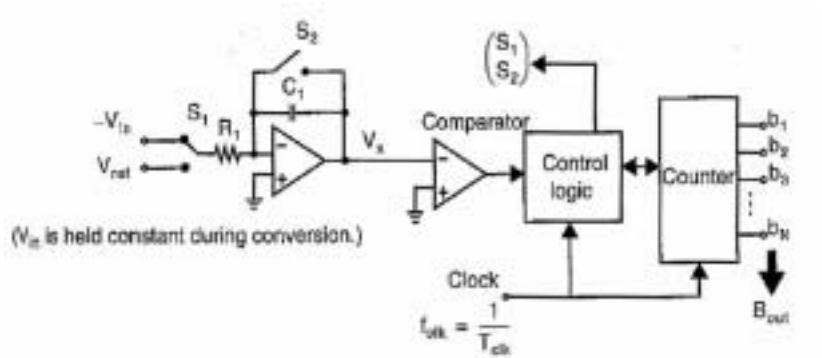


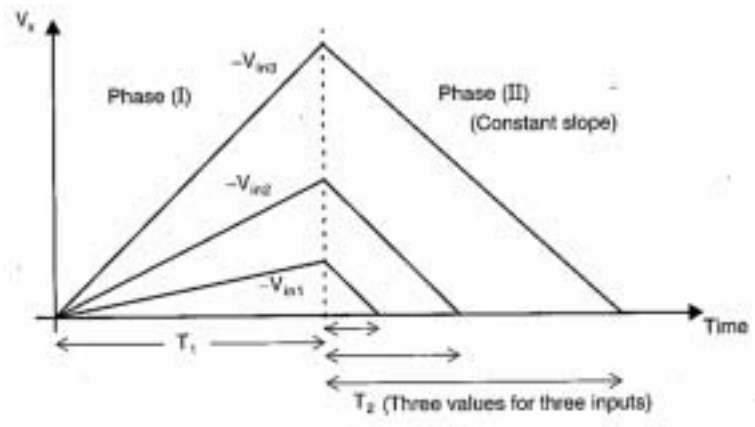


O. B. Milgrome, et al, "A 12 Bit Analog to Digital Converter for VLSI Applications in Nuclear Science," *IEEE Transactions on Nuclear Science*, Vol. 39, No. 4, pp. 771-5, 1992.

- Converts voltage into time interval
- N-bit conversion requires 2^N-1 clock cycles (worst case)
- Dual-edge clocked, Gray code counter improves speed performance
- Compact, low power
- Easily extended to multichannel systems
  - *counter, ramp generator common to all channels*
  - *Sample/hold, comparator, and output register per channel*

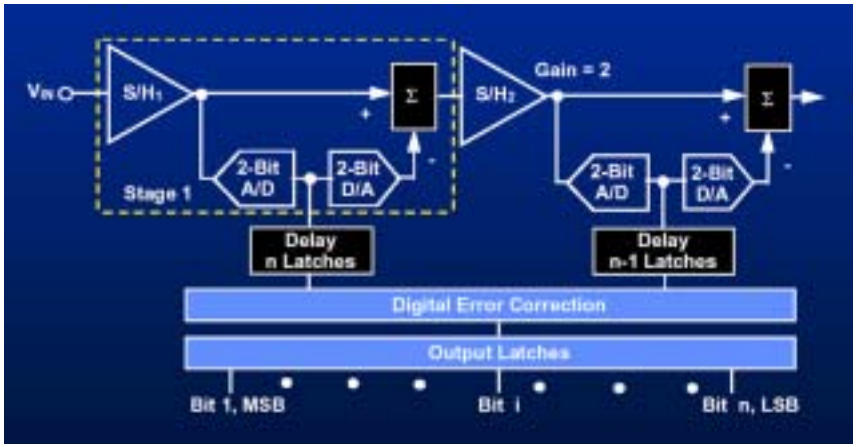
Dual-slope integrator





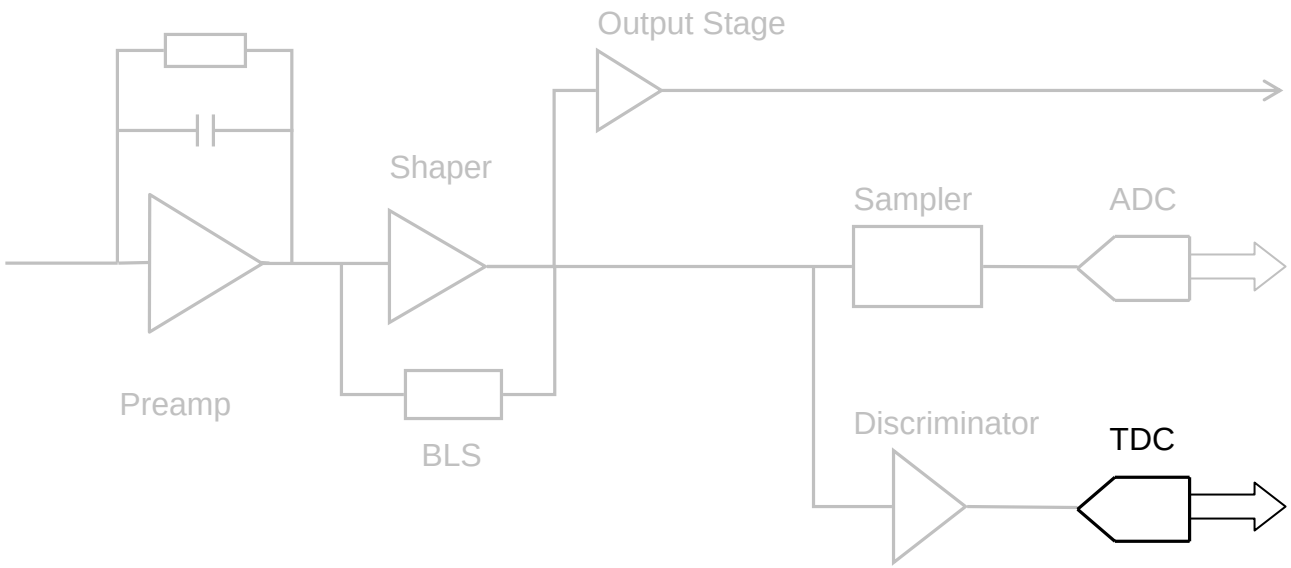
- Compare V_{in} to reference voltage by measuring time needed to charge/discharge C_1
- 2^N clock cycles per conversion, worst case
- Result independent of R_1,C_1, comparator offset
- Largely supplanted by oversampling Σ–Δ converters in most commercial markets

Pipeline converter

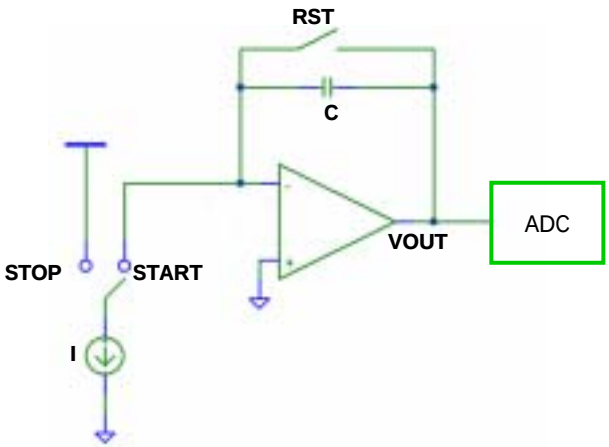


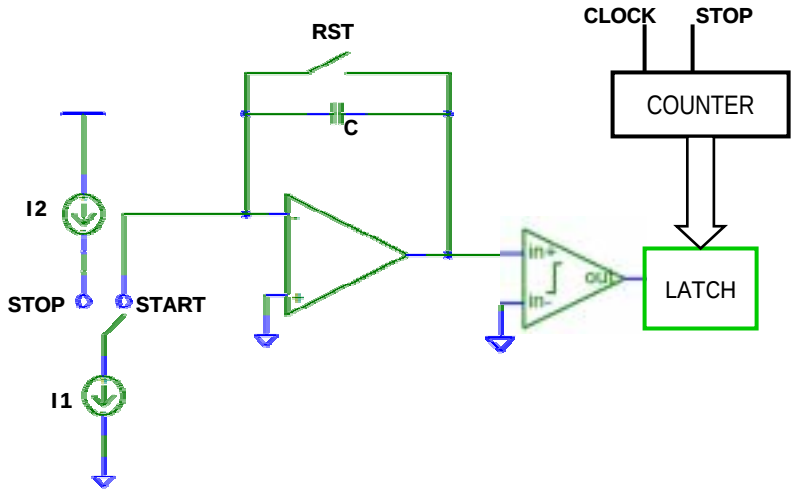
- Cascade of N stages, each stage consists of a sample/hold, low resolution ADC and DAC, summing amplifier with gain-of-2
- Each stage converts one bit and passes the residue on to the next stage
- N samples being simultaneously processed
- High throughput, moderate complexity, low power
- Only first stage needs full accuracy
- Sub-converter nonidealities can be removed by digital error correction
- Latency of N clocks between sample and valid data
- Minimum clock rate because of droop of internal S/H's
- Cannot be operated in burst mode

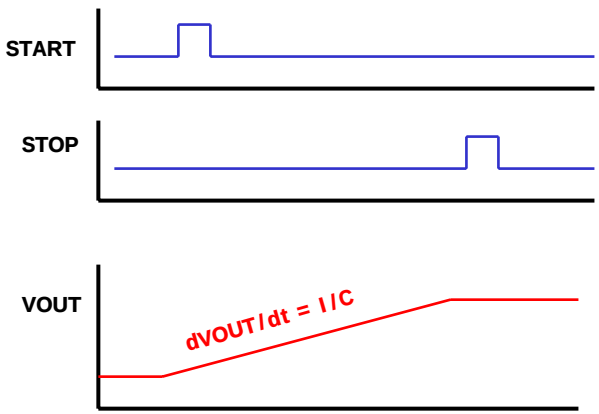
Time-to-digital converter (TDC)

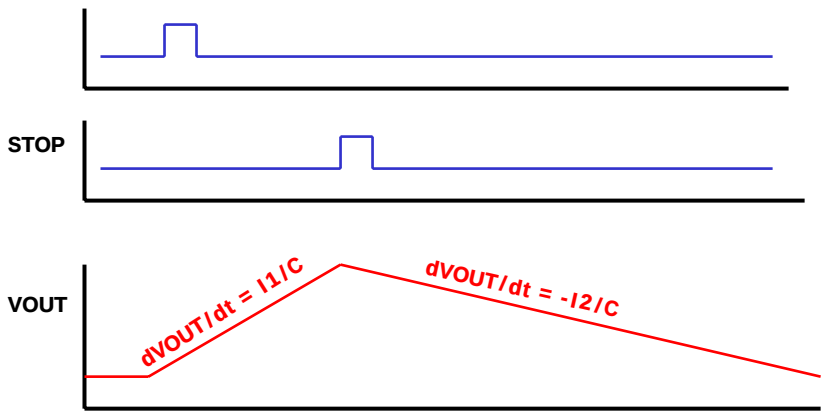


Time-to-amplitude converter (TAC)

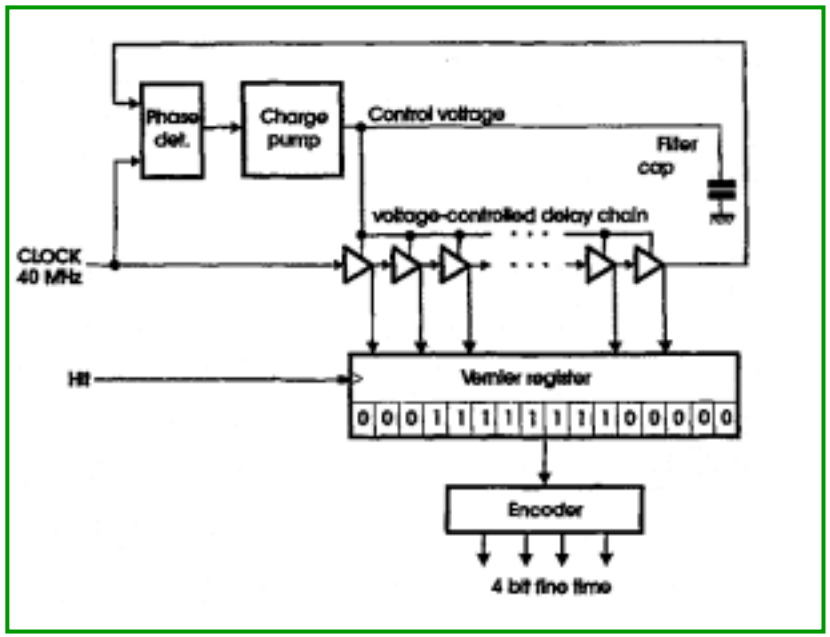






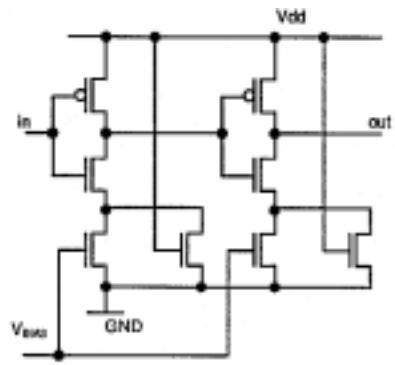


Delay-locked loop interpolator

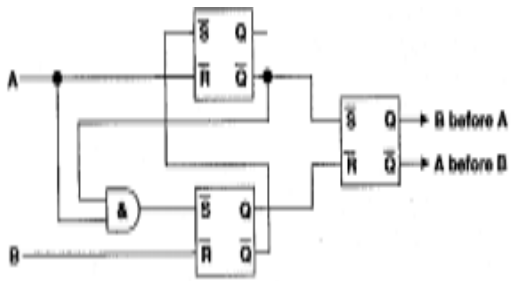


- Clock (START) signal propagated down a tapped, N-element delay chain
- Hit (STOP) freezes state of delay line
- Delay per stage stabilized to T_{ck}/N by phase-locking output to input, using voltage control of delay elements
- Resolution T_{ck}/N; dynamic range T_{ck}
- Extend dynamic range by coarse counter
- Mismatch of delay elements ➔ nonlinearity
- Long delay lines more nonlinear
- Easily extended to multichannel systems:
  - *DLL common to all channels*
  - *Latch, encoder per channel*

Variable delay element

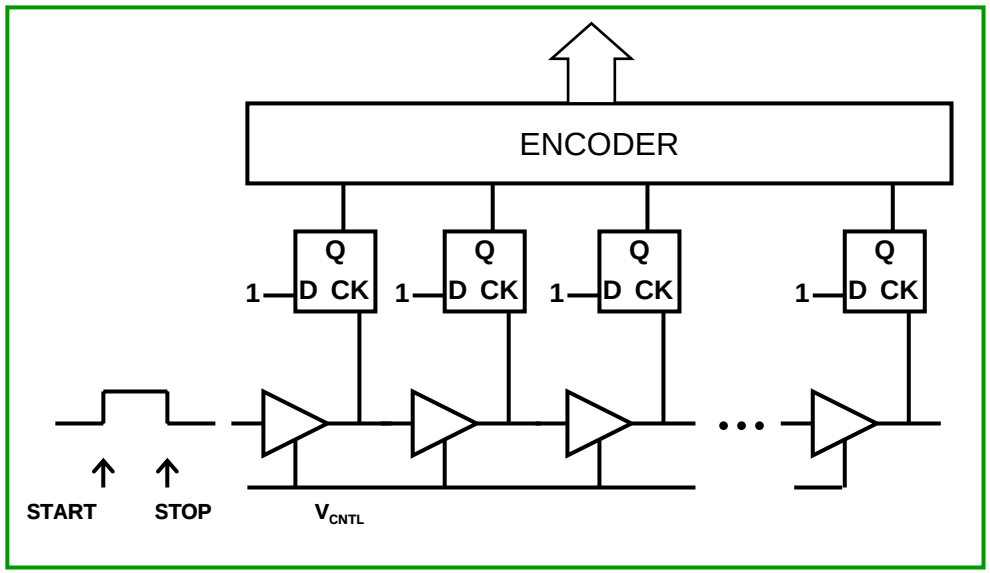


Phase detector



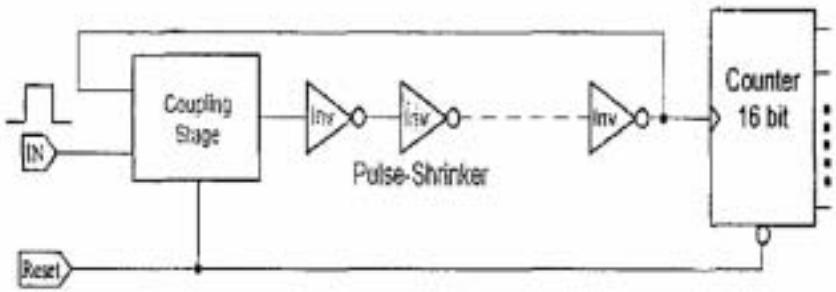
K. Barish et al., Nuclear Science Symposium Conference Digest IEEE, Nov. 2001, 604

Pulse-shrinking TDC



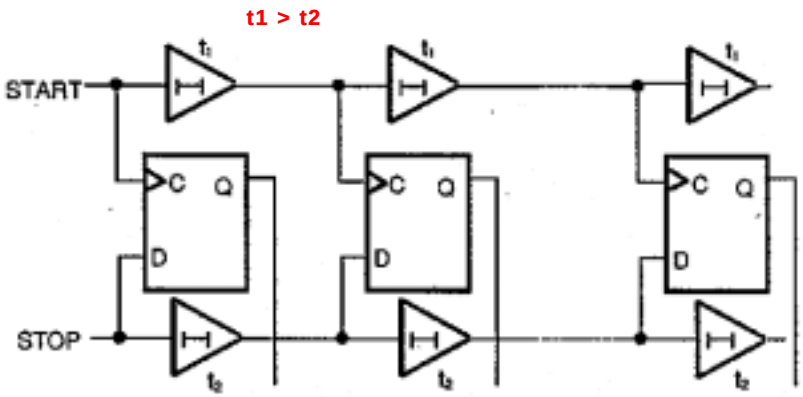
- Chain of pulse-shrinking elements
- Change of pulse width Δt per cell (stabilized)
- After n cells the pulse width shrinks to zero
- Cyclic version recirculates pulse through same shrinking element; count number of cycles until pulse vanishes
- Resolution LSB can be << t_{pd} of the technology
- Conversion time > time interval to be measured
- Both schemes can be combined with coarse counters to extend dynamic range

Cyclic version



E. Raisanen-Ruotsalainen, IEEE J. Solid State Circuits 30(9), 984 (1995)
S. Tisa et al., Proc. ISCAS 2003, p.465

Vernier DLL principle



- START and STOP signals propagate down separate delay lines
- START chain has longer element delay than STOP
- Measure the stage where STOP catches up to START
- Stabilize by controlling *difference* t1-t2 so that $N(t1-t2) = T_{ck}$
- Resolution LSB can be << t_{pd} of the technology

P. Dudek, IEEE Trans. Solid-State Circuits 35(2), 240 (2000)

Not in signal path, but important

- Power conditioning and distribution
- Bias circuits
- Electrostatic discharge protection
- Digital configuration switches
- Analog monitor
- DACs
  - *set comparator thresholds*
  - *trim channel-channel variations*
- Calibration pulser

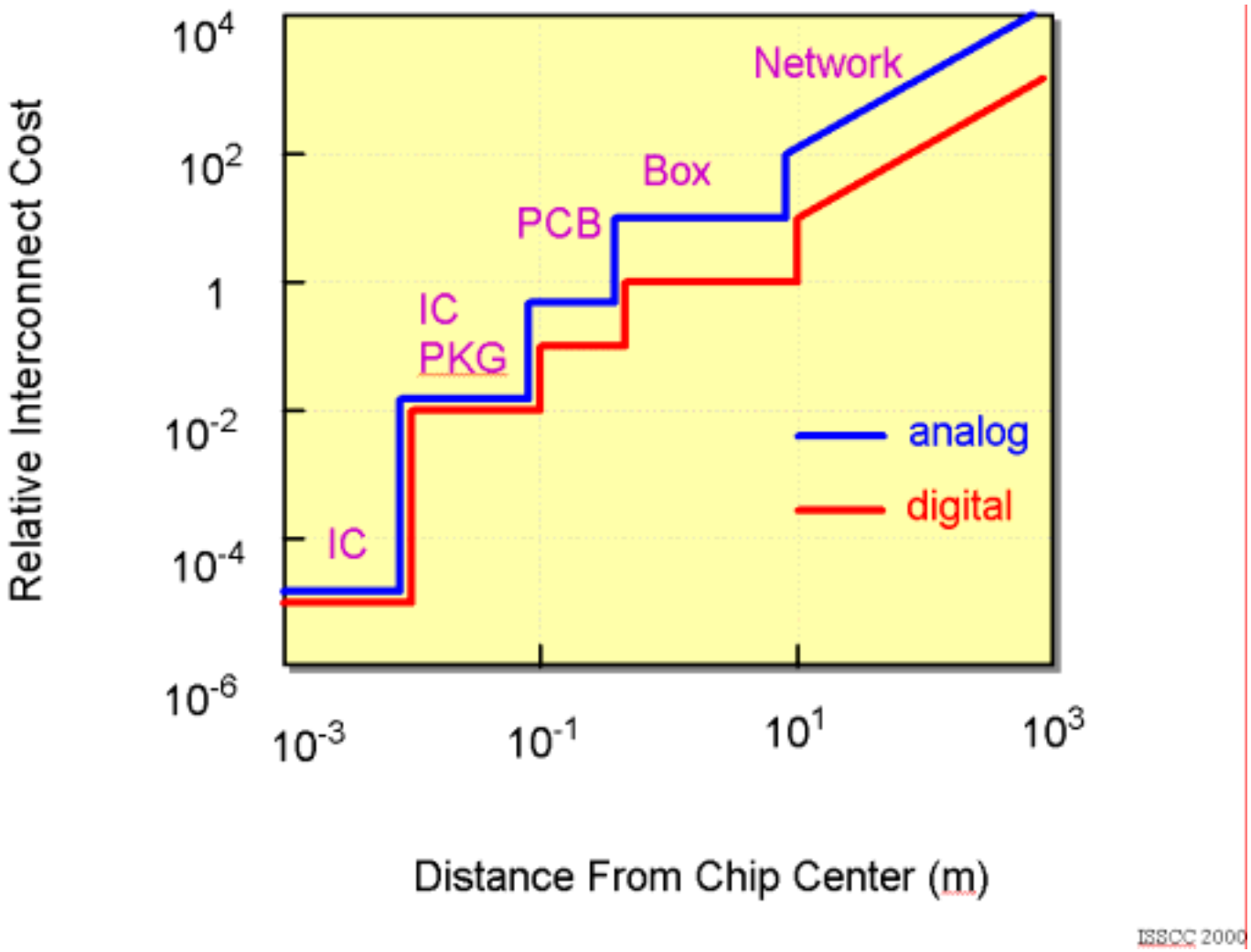
Packaging, Interconnect, and Systems Issues

Paul O'Connor, Brookhaven National Laboratory

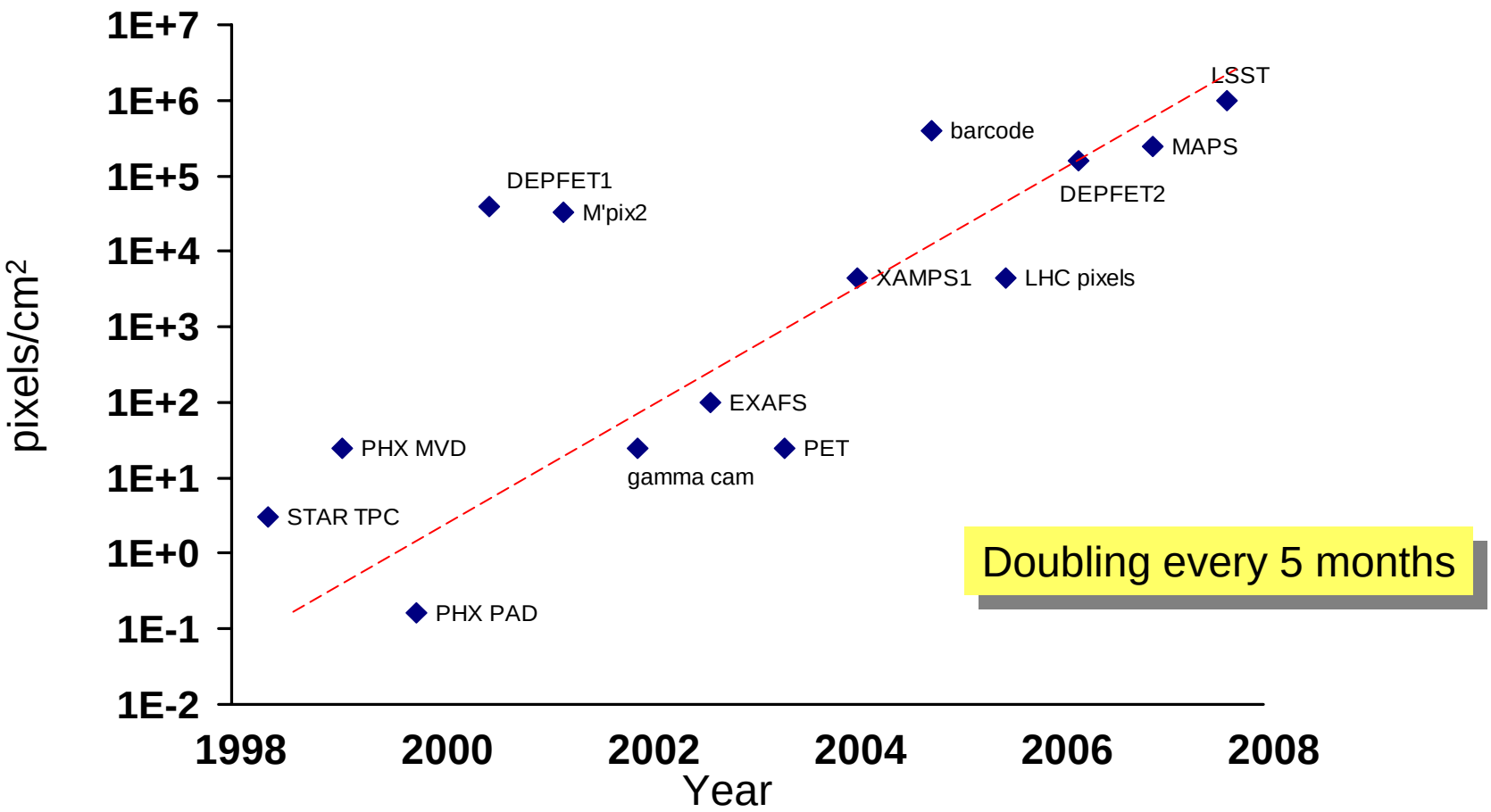
IEEE Nuclear Sciences Symposium/Medical Imaging Conference

October 24, 2009

Cost of interconnect



Pixel density

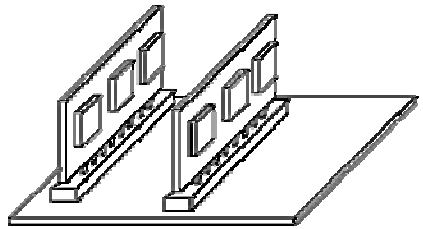


Interconnect issues in monolithic front ends

- Detector – Front End
  - Lowest possible capacitance for low noise
  - Maintain small form factor
  - Ease of assembly
- Front end – Data Acquisition
  - Analog processing to reduce the required level of digitization
    - *sampling*
    - *peak detection*
    - *multiplexing*
  - Efficient use of expensive “analog” interconnect

Detector – FE interconnect choices

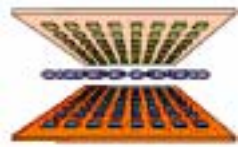
- **board-to-backplane**
  - easy to test, repair
  - large boards possible
  - connector pins are failure points
  - coarse pitch and high capacitance (> 1pF)



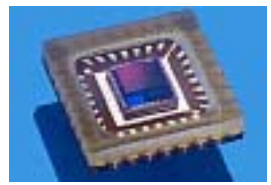
- **standard SMT package soldered to board (QFP or BGA)**
  - easy to test, difficult to repair
  - capacitance down to 0.2 pF for small packages
  - board area limited by reflow oven capacity

- **wirebonded chip-on-board**
  - difficult to test, assemble, and repair
  - board area limited by wirebonder
  - fragile
  - low capacitance (0.1 pF)

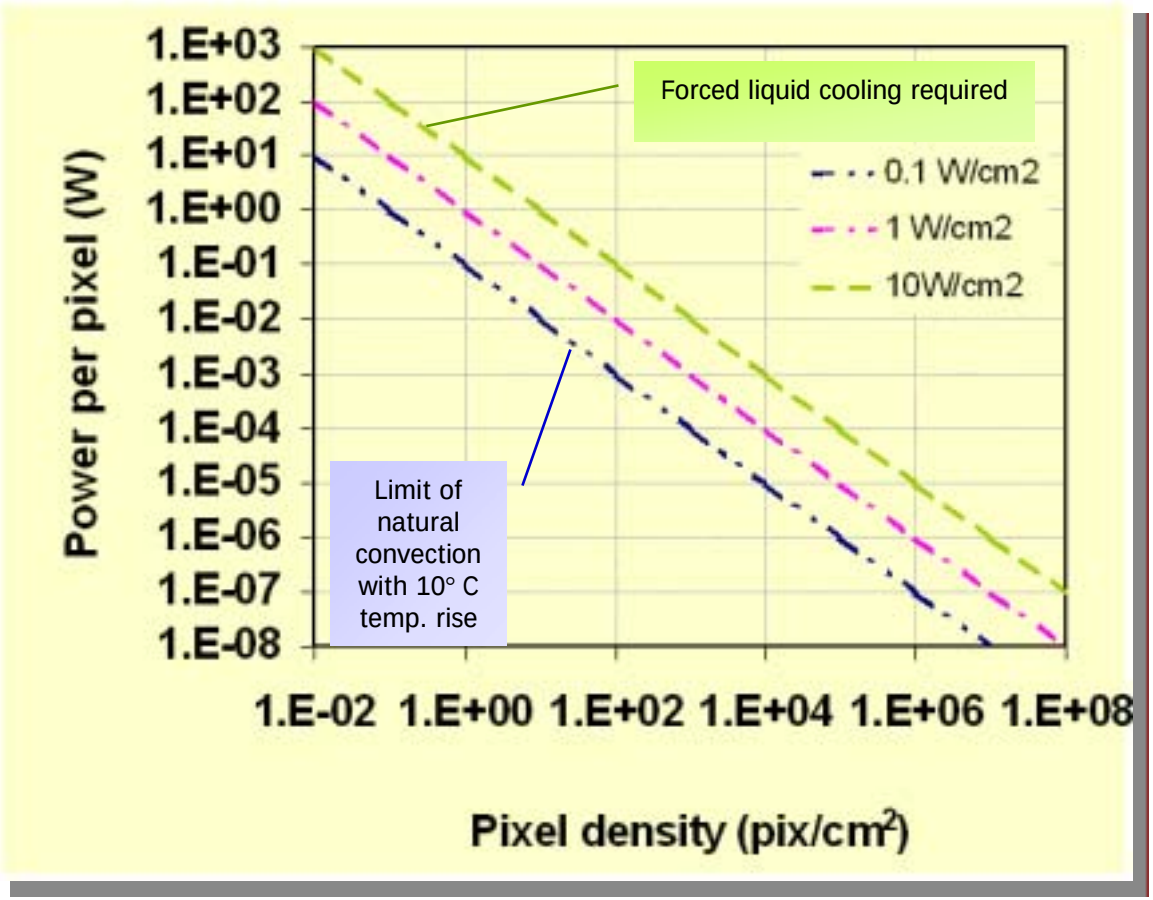
- **bump-bonded flip-chip**
  - can match pixels with pitch from ~30 – 1000 μm
  - difficult to test, assemble, and repair
  - circuitry has to fit in same area as pixel



- **monolithic detector/electronics**
  - interconnect is created as part of the detector fabrication process
  - ultra-low capacitance (few fF)

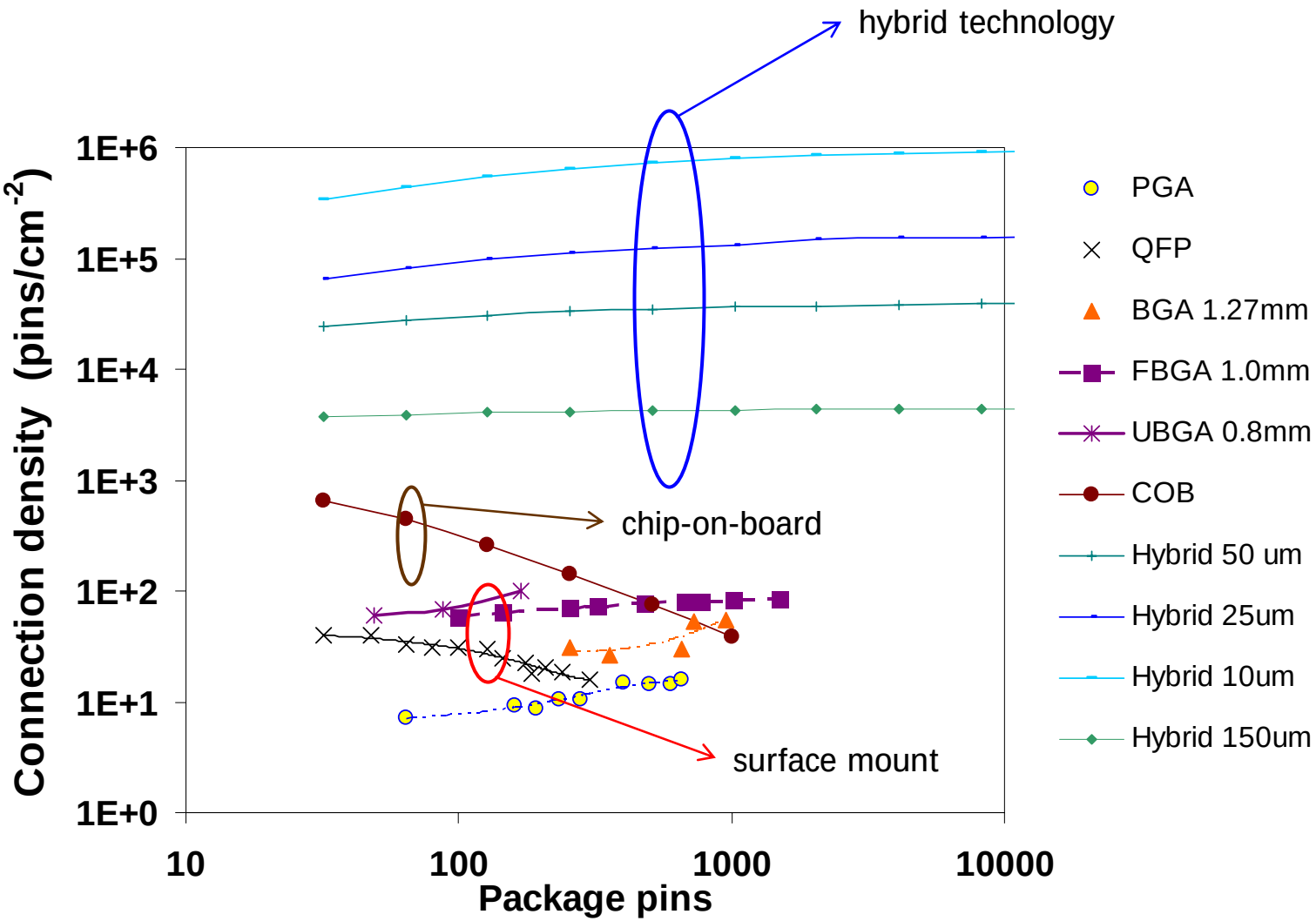


Power density



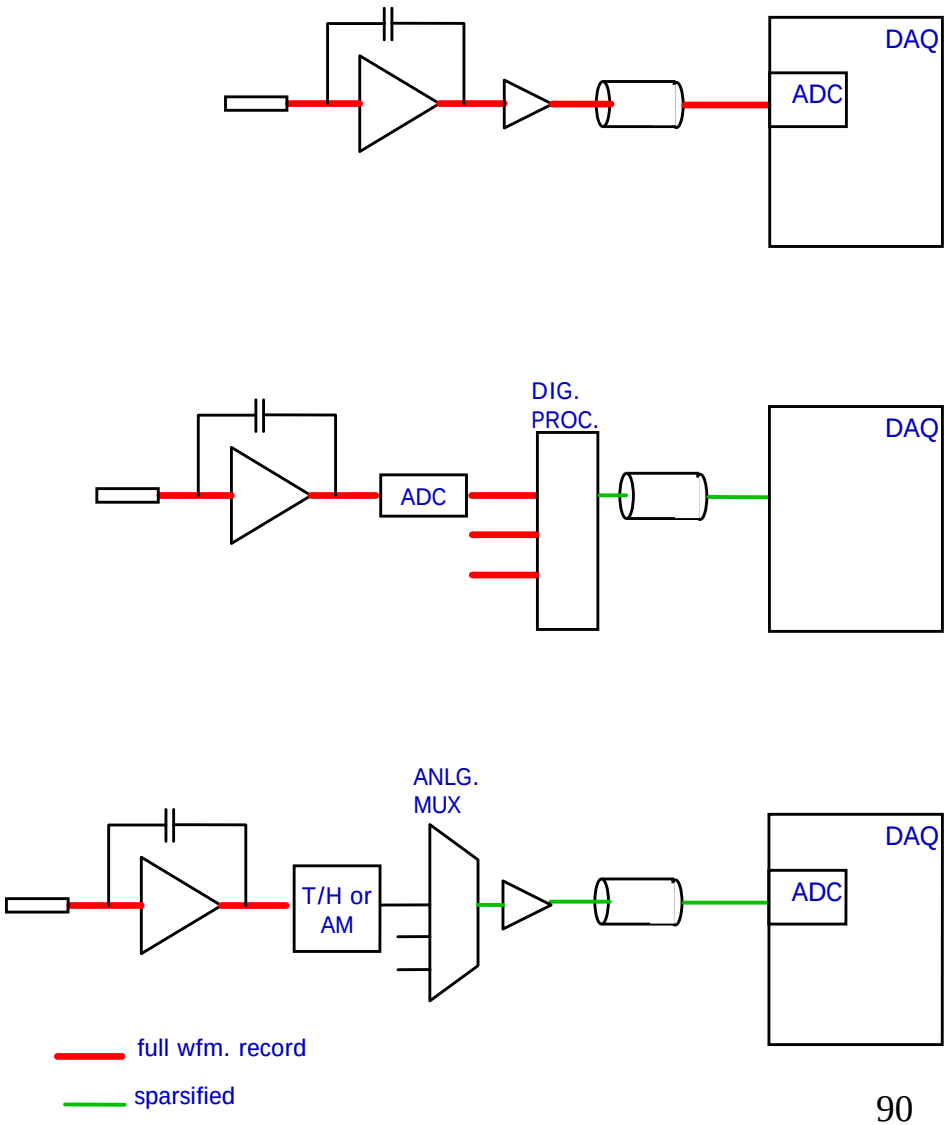
- On-detector power density is limited by cooling capability.
- Electronics for high-density detector must be extremely low power.

Packaging density

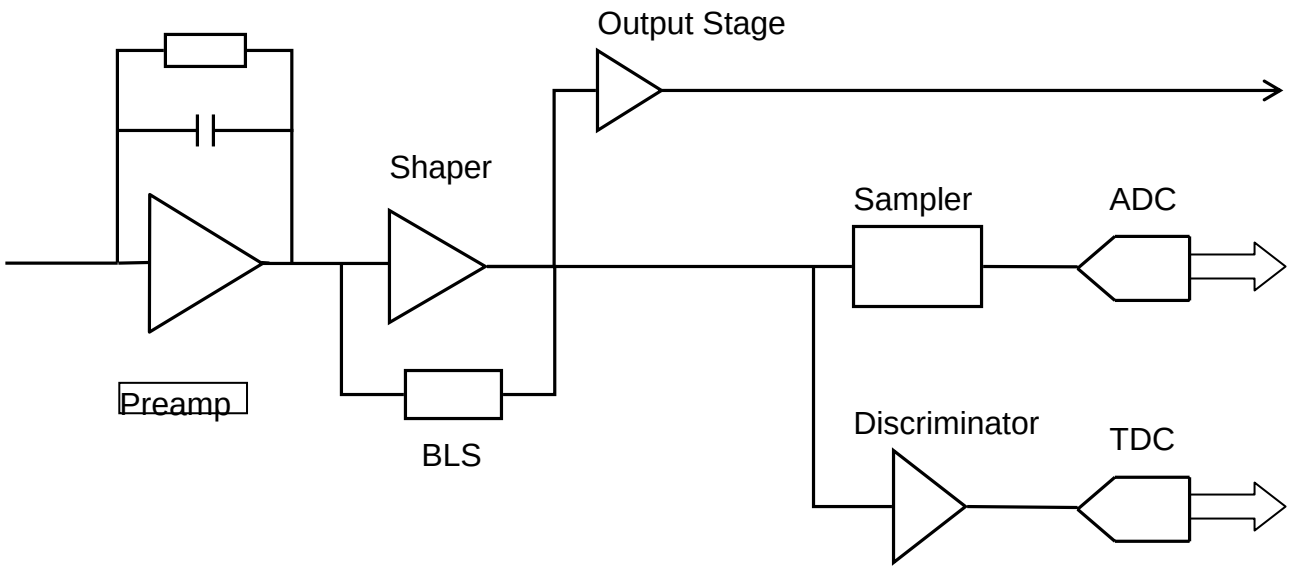


Front end – DAQ interconnect

- High bandwidth analog interconnect is expensive and bulky.
- Due to the low occupancy, this interconnect bandwidth is mostly wasted.
- Digitizing every channel is inefficient in a low-occupancy system.
- Existing approaches to sampling and multiplexing are inefficient:
  - *track/hold needs trigger, incurs deadtime during readout*
  - *analog memory (SCA) deadtimeless but needs trigger, multiple samples, no sparsification, complex controller*



Putting it all together



Power Efficient Architecture

- Highest power functions:
  - *charge preamplifier*
  - *analog line driver*
  - *ADC*

- Staying within a power budget and achieving maximum performance involves careful tradeoff.

Figure of merit for charge amplifiers and ADCs

$$FOM_{CSA} = \frac{P_d \cdot \tau_p}{Q_{\max} / \sigma_Q}$$

- Expresses the power cost of achieving SNR and speed
- Can be applied to front ends in any technology
- Corresponds to figure of merit for analog-digital converters:

$$FOM_{ADC} = \frac{P_d}{2^{ENOB} \cdot f_s}$$

Rule-of-thumb estimates

- Use FOM_{CSA} ~ 1pJ, calculate most quantities of interest.
- Given P_{max}, rate r, what is achievable SNR?

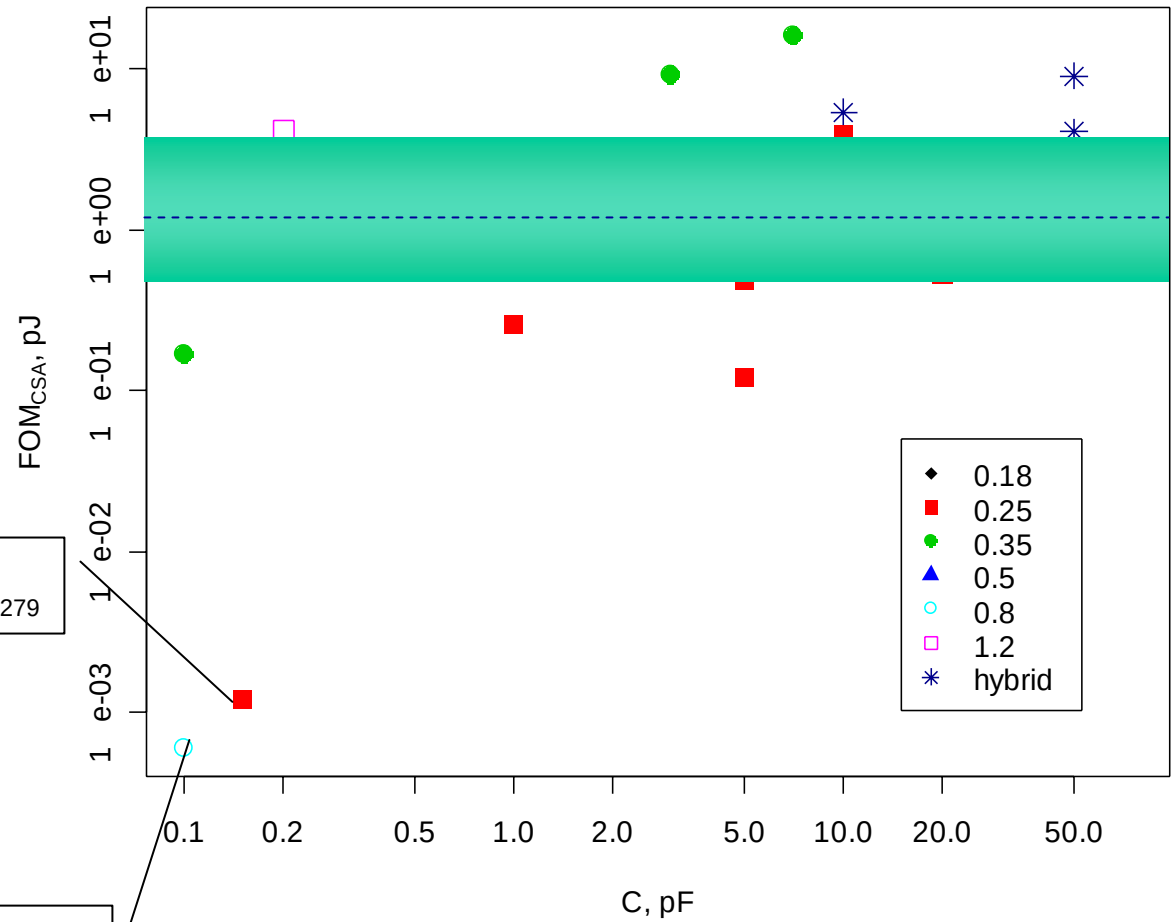
$$SNR = \frac{P}{FOM_{CSA} \cdot 10r}$$

  - *e.g.* P *=1mW,* r *=100kHz, SNR ~ 10^3*
- What power needed to get timing accuracy σ_t?

$$\sigma_t \approx \frac{\sigma_V}{dV/dt} \sim \frac{\tau_p}{SNR}; \quad P = \frac{FOM_{CSA}}{\sigma_t}$$

  - *e.g.* σ_t *=2ns,* P *~ 50μW*

Figure of merit for charge amplifiers (FOM_{CSA}) vs. detector capacitance

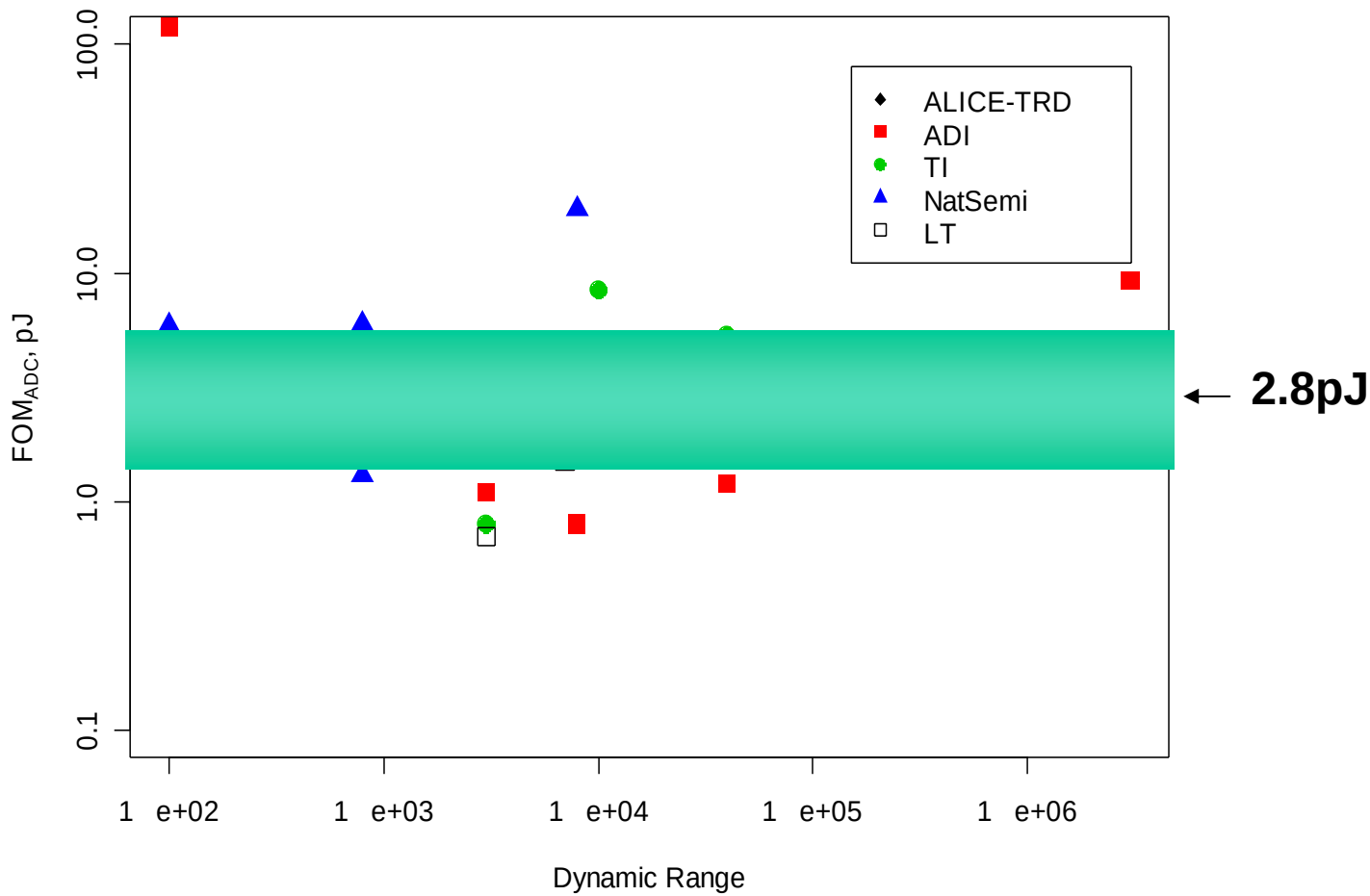


← 1.5pJ

Medipix-2
Llopart et al., TNS49(2002)2279

PSI-46
Erdmannt et al., NIMA549(2005)153

Figure of merit for ADCs (FOM_{ADC}) vs. dynamic range



Architecture choices

- Digital waveform recording of every channel requires ADC to have:
  - *same SNR as charge amplifier*
  - *sampling frequency 2X – 20X higher than analog bandwidth*
- **Guarantees** $P_{ADC} >> P_{CSA}$
- Better architecture: capture and buffer the analog information on the FEE ASIC, then steer samples to the ADC
- Switched capacitors or peak detectors can serve as the sampling cells
- Use analog buffers (memory) with simultaneous READ/WRITE to avoid deadtime

Example: TPC Digitization Power

- N_{pads} 8000
- $N_{timeslices}$ 500
- N_{voxels} $4x10^6$
- t_{drift} 7μs
- f_{trig} 2kHz
- Occupancy 2%

- Digitization Energy (12 bit resolution):
  - *10^{-12}J/bit * 2^{12} * N_{voxels} = 16 mJ*
- Power (FADC):
  - *16mJ / 7μs = 2000W (250 mW/chan)*
- Power (buffer and readout at 2 kHz trigger rate):
  - *16mJ / 500μs = 30W (4 mW/chan)*

• Compare with 0.75mW/chan for amplifier + 0.6mW/chan for PD + TAC.

• With sparsified readout of only occupied channels buffered in PD: P_{ADC} ~ 0.6W (75 μW/chan).

Summary

- Modern IC technologies, optimized for digital performance, are challenging for analog design but offer exceptional integration density, speed, and radiation tolerance.
- Noise is limited by available power, detector properties, event rate, and the 1/f properties of the technology.
- In addition to optimizing the first transistor, choice of shaping function is also important in noise optimization.
- High-order shapers improve the power/noise tradeoff, and also improve pileup and charge collection performance.
- An empirical figure of merit for charge amplifiers, analogous to that for ADCs, can be used to guide design choices.
- Reducing the number of analog-to-digital conversions and minimizing off-chip analog signal transmission (where possible) improves noise by allowing power to be allocated to the front end.